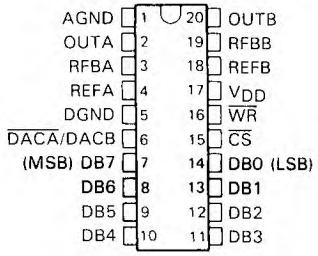
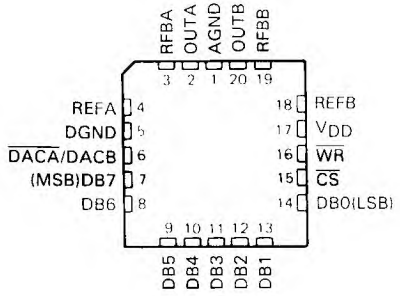
- **Advanced LinCMOS™ Silicon-Gate Technology**
- **Easy Microprocessor Interface**
- **On-Chip Data Latches**
- **Digital Inputs are TTL-Compatible with 10.8-V to 15.75-V Power Supply**
- **Monotonic Over the Entire A/D Conversion Range**
- **Designed to be Interchangeable with Analog Devices AD7628**
- **Fast Control Signaling for Digital Signal Processor Applications Including Interface with TMS320**

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



KEY PERFORMANCE SPECIFICATIONS	
Resolution	8 bits
Linearity Error	1/2 LSB
Power Dissipation at V_{DD} = 15 V	15 mW
Settling Time at V_{DD} = 5 V	100 ns
Propagation Delay at V_{DD} = 5 V	80 ns

description

The AD7628 is a dual 8-bit digital-to-analog converter designed with separate on-chip data latches and featuring excellent DAC-to-DAC matching. Data is transferred to either of the two DAC data latches via a common 8-bit input port. Control input $\overline{DACA}$/DACB determines which DAC is loaded. The "load" cycle of the AD7628 is similar to the "write" cycle of a random-access memory, allowing easy interface to most popular microprocessor busses and output ports. Segmenting the high-order bits minimizes glitches during changes in the most significant bits, where glitch impulse is typically the strongest.

The AD7628 operates from a 10.8-V to 15.75-V power supply and is TTL-compatible over this range. Power dissipation is less than 15 mW. Excellent 2- or 4-quadrant multiplying makes the AD7628 a sound choice for many microprocessor-controlled gain-setting and signal-control applications.

The AD7628B is characterized for operation from −25°C to 85°C. The AD7628K is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

SYMBOLIZATION		OPERATING
DEVICE	PACKAGE SUFFIX	TEMPERATURE RANGE
AD7628B	FN, N	−25°C to 85°C
AD7628K	FN, N	0°C to 70°C

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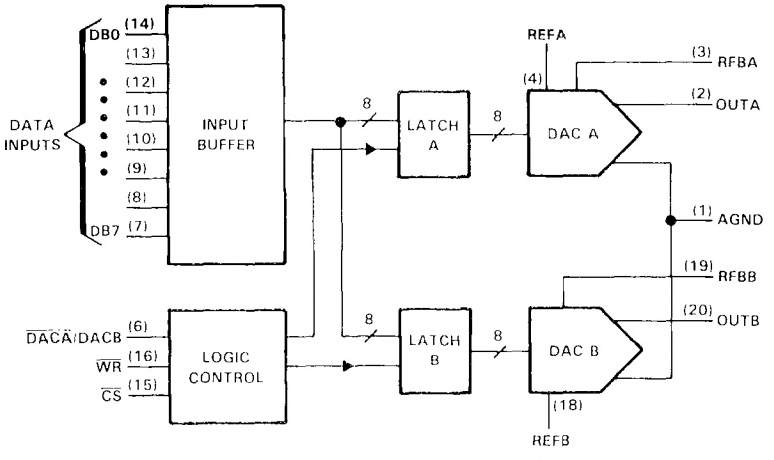
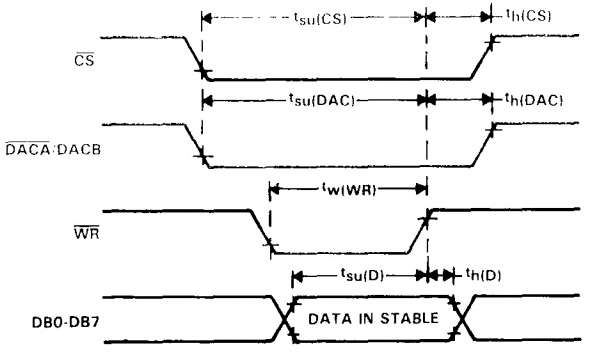
functional block diagram



operating sequence



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (to AGND or DGND) . . . . . −0.3 V to 17 V
Voltage between AGND and DGND . . . . . $\pm V_{DD}$
Input voltage, V_I (to DGND) . . . . . −0.3 V to V_{DD} +0.3 V
Reference voltage, V_{refA} or V_{refB} (to AGND) . . . . . ±25 V
Feedback voltage, V_{RFBA} or V_{RFBB} (to AGND) . . . . . ±25 V
Output voltage, V_{OA} or V_{OB} (to AGND) . . . . . ±25 V
Peak input current . . . . . 10 μA
Operating free-air temperature range: AD7628B . . . . . −25°C to 85°C
AD7628K . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		10.8		15.75	V
Reference voltage, V_{refA} or V_{refB}			±10		V
High-level input voltage, V_{IH}		2.4			V
Low-level input voltage, V_{IL}				0.8	V
$\overline{CS}$ setup time, $t_{su(CS)}$		50			ns
$\overline{CS}$ hold time, $t_{h(CS)}$		0			ns
DAC select setup time, $t_{su(DAC)}$		50			ns
DAC select hold time, $t_{h(DAC)}$		10			ns
Data bus input setup time $t_{su(D)}$		25			ns
Data bus input [illegible] time $t_{h(D)}$		0			ns
Pulse duration, [illegible]ow, $t_{w(WR)}$		50			ns
Operating free-air temperature, T_A	AD7628B	−25		85	°C
	AD7628K	0		70	

3 Product Previews

electrical characteristics over recommended ranges of operating free-air temperature and V_{DD}, V_{refA} = V_{refB} = 10 V, V_{OA} and V_{OB} at 0 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	MAX	UNIT
I_{IH}	High-level input current		$V_I = V_{DD}$	Full Range		10	μA
				25°C		1	
I_{IL}	Low-level input current		$V_I = 0$	Full Range		−10	μA
				25°C		−1	
	Reference input impedance (Pin 15 to GND)				8	15	kΩ
I_{lkg}	Output leakage current	OUTA	DAC data latch loaded with 00000000, V_{refA} = ±10 V	Full Range		±200	nA
				25°C		±50	
		OUTB	DAC data latch loaded with 00000000, V_{refB} = ±10 V	Full Range		±200	
				25°C		±50	
	Input resistance match (REFA to REFB)					±1%	
	DC supply sensitivity $\Delta gain/\Delta V_{DD}$		ΔV_{DD} = ±5%	Full Range		0.02	%/%
				25°C		0.01	
I_{DD}	Supply current	Quiescent	DB0-DB7 at V_{IH}min or V_{IL}max			1	mA
		Standby	DB0-DB7 at 0 V or V_{DD}	Full Range		0.5	
				25°C		0.1	
C_i	Input capacitance	DB0-DB7	V_I = 0 or V_{DD}			10	pF
		$\overline{WR}$, $\overline{CS}$, $\overline{DACA}$/DACB				15	
C_o	Output capacitance (OUTA, OUTB)		DAC Data latches loaded with 00000000			25	pF
			DAC Data latches loaded with 11111111			60	

3 Product Previews

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operating characteristics over recommended ranges of operating free-air temperature and V_{DD}, $V_{refA} = V_{refB} = 10$ V, V_{OA} and V_{OB} at 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Linearity error						±1/2	LSB
Setting time (to 1/2 LSB)		See Note 1				100	ns
Gain error		See Note 2	Full Range			±3	LSB
			25°C			±2	
AC feedthrough	REFA to OUTA	See Note 3	Full Range			−65	dB
	REFB to OUTB		25°C			−70	
Temperature coefficient of gain						0.0035	%FSR/°C
Propagation delay (from digital input to 90% of final analog output current)		See Note 4				80	ns
Channel-to-channel isolation	REFA to OUTB	See Note 5	25°C		80		dB
	REFB to OUTA	See Note 6	25°C		80		
Digital-to-analog glitch impulse area		Measured for code transition from 00000000 to 11111111, T_A = 25°C			440		nV•s
Digital crosstalk glitch impulse area		Measured for code transition from 00000000 to 11111111, T_A = 25°C			60		nV•s
Harmonic distortion		V_i = 6 V, f = 1 kHz, T_A = 25°C			−85		dB

NOTES: 1. OUTA, OUTB load = 100 Ω, C_{ext} = 13 pF; $\overline{WR}$ and $\overline{CS}$ at 0 V; DB0-DB7 at 0 V to V_{DD} or V_{DD} to 0 V.
2. Gain error is measured using an internal feedback resistor. Nominal Full Scale Range (FSR) = V_{ref} − 1 LSB. Both DAC latches are loaded with 11111111.
3. V_{ref} = 20 V peak-to-peak, 10-kHz sine wave.
4. $V_{refA} = V_{refB}$ = 10 V; OUTA/OUTB load = 100 Ω, C_{ext} = 13 pF; $\overline{WR}$ and $\overline{CS}$ at 0 V; DB0-DB7 at 0 V to V_{DD} or V_{DD} to 0 V.
5. V_{refA} = 20 V peak-to-peak, 10-kHz sine wave; V_{refB} = 0.
6. V_{refB} = 20 V peak-to-peak, 10-kHz sine wave; V_{refA} = 0.

principles of operation

The AD7628 contains two identical 8-bit multiplying D/A converters, DACA and DACB. Each DAC consists of an inverted R-2R ladder, analog switches, and input data latches. Binary-weighted currents are switched between DAC output and AGND, thus maintaining a constant current in each ladder leg independent of the switch state. Most applications require only the addition of an external operational amplifier and voltage reference. A simplified D/A circuit for DACA with all digital inputs low is shown in Figure 1.

Figure 2 shows the DACA equivalent circuit. A similar equivalent circuit can be drawn for DACB. Both DACs share the analog ground pin 1 (AGND). With all digital inputs high, the entire reference current flows to OUTA. A small leakage current (I_{lkg}) flows across internal junctions, and as with most semiconductor devices, doubles every 10°C. C_O is due to the parallel combination of the NMOS switches and has a value that depends on the number of switches connected to the output. The range of C_O is 25 pF to 60 pF maximum. The equivalent output resistance r_O varies with the input code from 0.8R to 3R where R is the nominal value of the ladder resistor in the R-2R network.

Interfacing the AD7628 to a microprocessor is accomplished via the data bus, $\overline{CS}$, $\overline{WR}$, and $\overline{DACA}$/DACB control signals. When $\overline{CS}$ and $\overline{WR}$ are both low, the AD7628 analog output, specified by the $\overline{DACA}$/DACB control line, responds to the activity on the DB0-DB7 data bus inputs. In this mode, the input latches are transparent and input data directly affects the analog output. When either the $\overline{CS}$ signal or $\overline{WR}$ signal goes high, the data on the DB0-DB7 inputs is latched until the $\overline{CS}$ and $\overline{WR}$ signals go low again. When $\overline{CS}$ is high, the data inputs are disabled, regardless of the state of the $\overline{WR}$ signal.

The digital inputs of the AD7628 provide TTL compatibility when operated from a supply voltage of 10.8 V to 15.75 V. Power dissipation is a low 10 mW within this range.

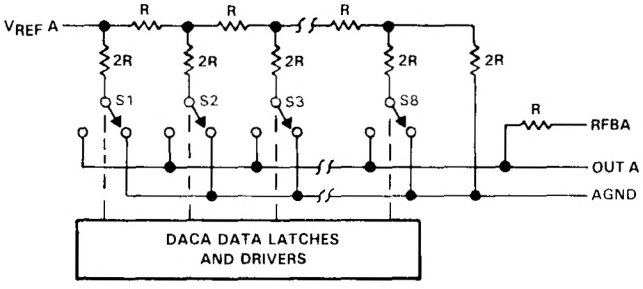

FIGURE 1. SIMPLIFIED FUNCTIONAL CIRCUIT FOR DACA

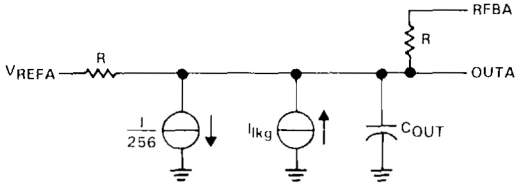

FIGURE 2. AD7628 EQUIVALENT CIRCUIT, DACA LATCH LOADED WITH 11111111.

MODE SELECTION TABLE

$\overline{DACA}$, DACB	$\overline{CS}$	$\overline{WR}$	DACA	DACB
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

L = low level, H = high level, X = don't care

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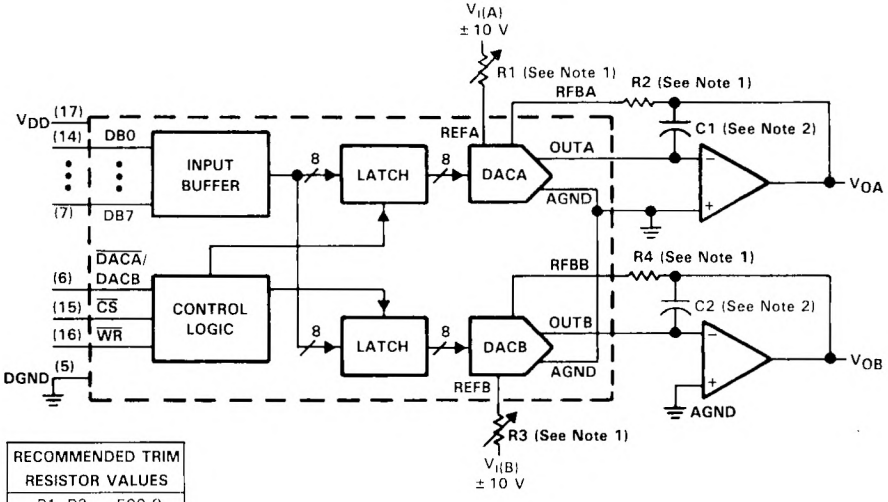
TYPICAL APPLICATION DATA

The AD7628 is capable of performing 2-quadrant or full 4-quadrant multiplication. Circuit configurations for 2-quadrant and 4-quadrant multiplication are shown in Figures 3 and 4. Input coding for unipolar and bipolar operation are summarized in Tables 1 and 2, respectively.

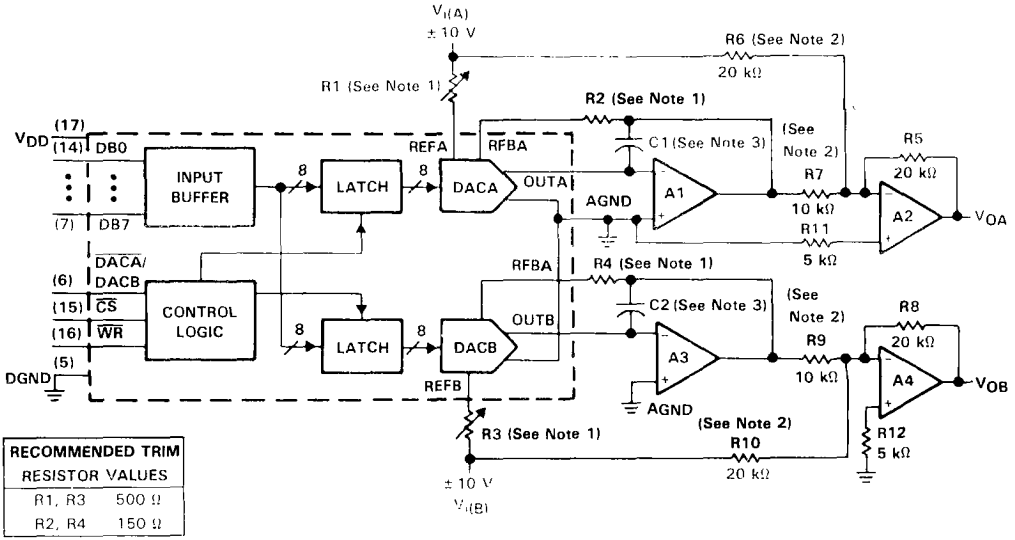


RECOMMENDED TRIM RESISTOR VALUES	
R1, R3	500 Ω
R2, R4	150 Ω

NOTES: 1. R1, R2, R3, and R4 are used only if gain adjustment is required. See table for recommended values. Make gain adjustment with digital input of 255.
2. C1 and C2 phase compensation capacitors (10 pF to 15 pF) are required when using high-speed amplifiers to prevent ringing or oscillation.

FIGURE 3. UNIPOLAR OPERATION (2-QUADRANT MULTIPLICATION)

TYPICAL APPLICATION DATA



RECOMMENDED TRIM RESISTOR VALUES	
R1, R3	500 Ω
R2, R4	150 Ω

NOTES: 1. R1, R2, R3, and R4 are used only if gain adjustment is required. See table in Figure 3 for recommended values. Adjust R1 for V_{OA} = 0 V with code 10000000 in DACA latch. Adjust R3 for V_{OB} = 0 V with 10000000 in DACB latch.
2. Matching and tracking are essential for resistor pairs R6, R7, R9, and R10.
3. C1 and C2 phase compensation capacitors (10 pF to 15 pF) may be required if A1 and A3 are high-speed amplifiers.

FIGURE 4. BIPOLAR OPERATION (4-QUADRANT OPERATION)

TABLE 1. UNIPOLAR BINARY CODE

DAC LATCH CONTENTS MSB LSB†	ANALOG OUTPUT
11111111	$-V_i$ (255/256)
10000001	$-V_i$ (129/256)
10000000	$-V_i$ (128/256) = $-V_i/2$
01111111	$-V_i$ (127/256)
00000001	$-V_i$ (1/256)
00000000	$-V_i$ (0/256) = 0

† 1 LSB = $(2^{-8})V_i$

TABLE 2. BIPOLAR (OFFSET BINARY) CODE

DAC LATCH CONTENTS MSB LSB‡	ANALOG OUTPUT
11111111	V_i (127/128)
10000001	V_i (1/128)
10000000	0 V
01111111	$-V_i$ (1/128)
00000001	$-V_i$ (127/128)
00000000	$-V_i$ (128/128)

‡ 1 LSB = $(2^{-7})V_i$

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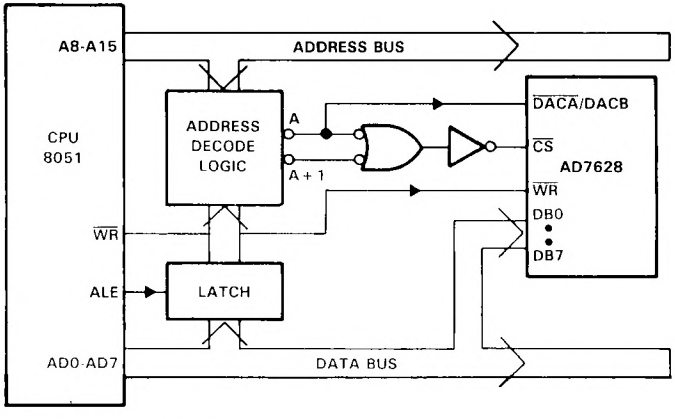
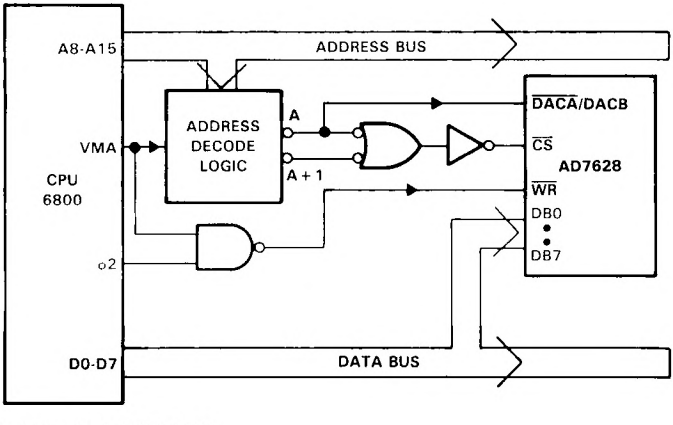
TYPICAL APPLICATION DATA

microprocessor interface information



NOTE: A = decoded address for AD7628 DACA.
A + 1 = decoded address for AD7628 DACB.

FIGURE 5. AD7628 — INTEL 8051 INTERFACE



NOTE: A = decoded address for AD7628 DACA.
A + 1 = decoded address for AD7628 DACB.

FIGURE 6. AD7628 — 6800 INTERFACE

TYPICAL APPLICATION DATA

voltage-mode operation

The AD7628 current-multiplying D/A converter can be operated in a voltage mode. In the voltage mode, a fixed voltage is placed on the current output pin. The analog output voltage is then available at the reference voltage pin. An example of a current-multiplying D/A converter operating in voltage mode is shown in Figure 7. The relationship between the fixed input voltage and the analog output voltage is given by the following equation:

$$\text{Analog output voltage} = \text{fixed input voltage } (D/256)$$

where D = the digital input. In voltage-mode operation, the AD7628 meets the following specification:

LINEARITY ERROR	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analog output voltage for REFA, B	V_{DD} = 12 V, OUTA or OUTB = 5 V, T_A = 0°C to 70°C			1	LSB

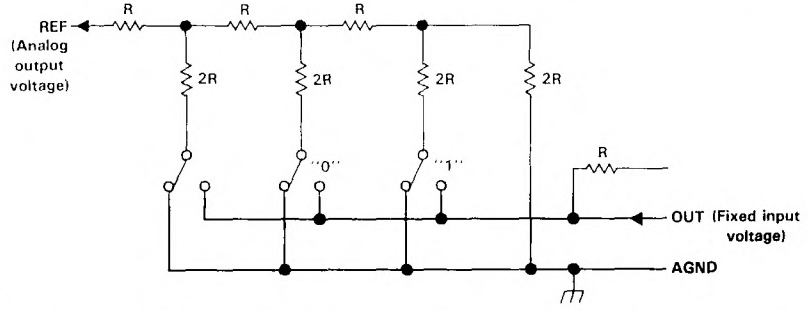


FIGURE 7. CURRENT-MULTIPLYING D/A CONVERTER OPERATING IN VOLTAGE MODE

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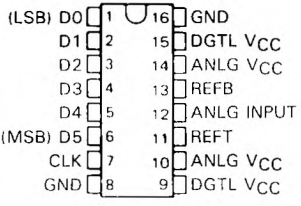
D3163, OCTOBER 1988

- 6-Bit Resolution
- 0.8% Linearity
- Maximum Conversion Rate . . . 25 MHz Typ
  20 MHz Min
- Analog Input Voltage Range . . .
  V_{CC} to V_{CC} – 2 V
- Analog Input Dynamic Range . . . 1 V
- TTL Digital I/O Level
- Low Power Consumption . . . 200 mW Typ
- 5-V Single-Supply Operation
- Interchangeable with Fujitsu MB40576

N PACKAGE
(TOP VIEW)

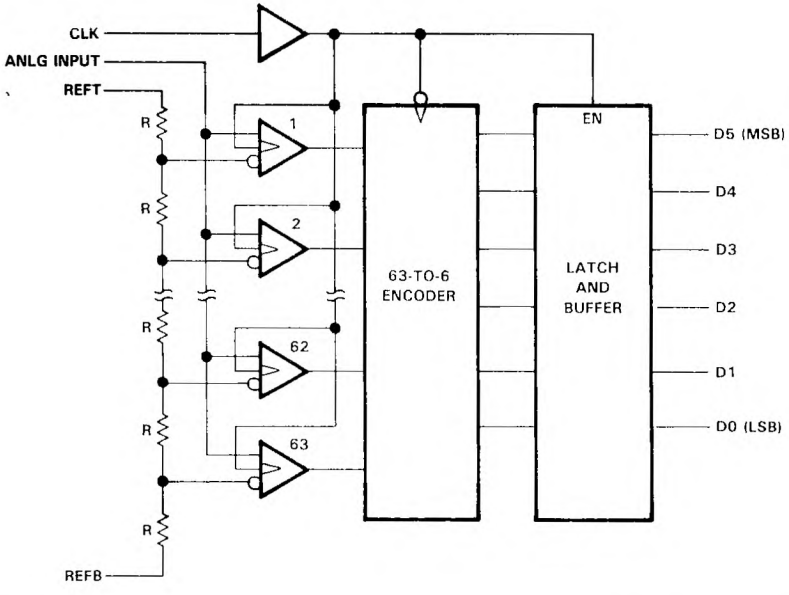


description

The TL5501 is a low-power ultra-high-speed video-band analog-to-digital converter that uses the Advanced Low-Power Schottky (ALS) process. It utilizes the full-parallel comparison (flash method) for high-speed conversion. It converts wide-band analog signals (such as a video signal) to a digital signal at a sampling rate of dc to 25 MHz. Because of such high-speed capability, the TL5501 is suitable for digital video applications such as digital TV, video processing with a computer, or radar signal processing.

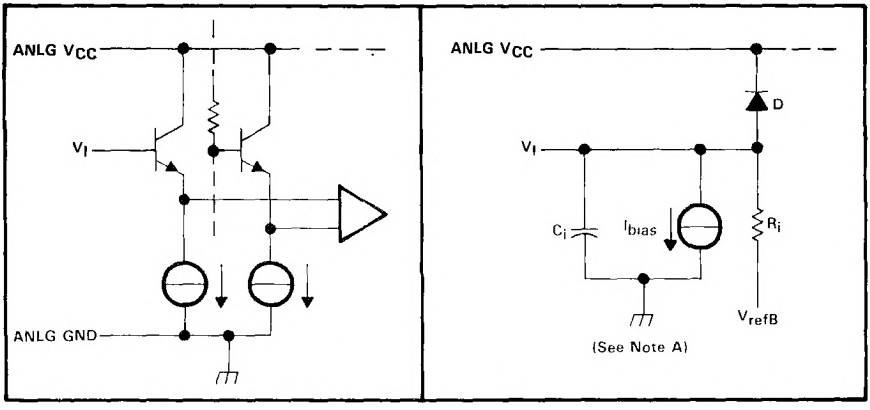
The TL5501 is characterized for operation from 0°C to 70°C.

functional block diagram



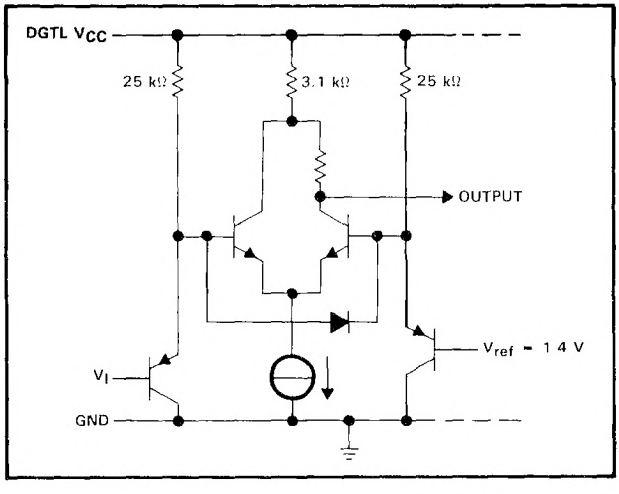
3 Product Previews

equivalents of analog input circuit



NOTE A: C_i — nonlinear emitter-follower junction capacitance
R_i — linear resistance model for input current transition caused by comparator switching. $V_I < V_{refB}$: Infinite; CLK high: Infinite.
V_{refB} — voltage at REFB terminal
I_{bias} — constant input bias current
D — Base-collector junction diode of emitter-follower transistor

equivalent of digital input circuit



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FUNCTION TABLE

STEP	ANALOG INPUT VOLTAGE†	DIGITAL OUTPUT CODE
0	3.992 V	L L L L L L
1	4.008 V	L L L L L H
⋮	⋮	⋮
31	4.488 V	L H H H H H
32	4.508 V	H L L L L L
33	4.520 V	H L L L L H
⋮	⋮	⋮
62	4.984 V	H H H H H L
63	5.000 V	H H H H H H

† These values are based on the assumption that V_{refB} and V_{refT} have been adjusted so that the voltage at the transition from digital 0 to 1 (V_{ZT}) is 4.000 V and the transition to full scale (V_{FT}) is 4.992 V. 1 LSB = 16 mV.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, ANLG V_{CC} . . . . . −0
Supply voltage range, DGTL V_{CC} . . . . . −0
Input voltage range at digital input, V_I . . . . . −0.5 V to 7 V
Input voltage range at analog input, V_I . . . . . −0.5 V to ANLG V_{CC} +0.5 V
Analog reference voltage range, V_{ref} . . . . . −0.5 V to ANLG V_{CC} +0.5 V
Storage temperature range . . . . . −55°C to 150°C
Operating free-air temperature range . . . . . 0°C to 70°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, ANLG V_{CC}	4.75	5	5.25	V
Supply voltage, DGTL V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Input voltage at analog input, V_I (see Note 1)	4		5	V
Analog reference voltage (top side), V_{refT} (see Note 1)	4	5	5.1	V
Analog reference voltage (bottom side), V_{refB} (see Note 1)	3	4	4.1	V
High-level output current, I_{OH}			−400	μA
Low-level output current, I_{OL}			4	mA
Clock pulse duration, high-level or low-level, t_w	25			ns
Operating free-air temperature, T_A	0		70	°C

NOTE 1: $V_{refB} < V_I < V_{refT}$, $V_{refT} - V_{refB} = 1$ V ± 0.1 V.

electrical characteristics over operating supply voltage range, T_A = 25°C (unless otherwise noted)

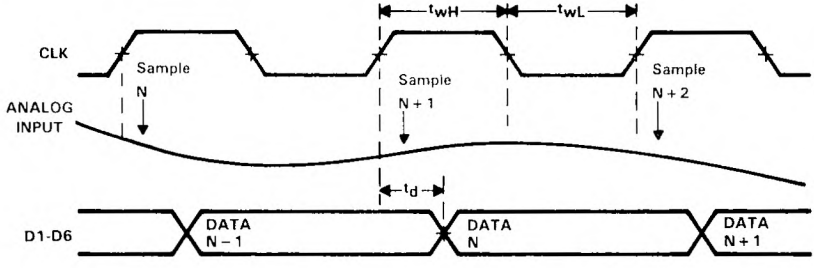
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_I	Analog input current	V_I = 5 V			75	μA
		V_I = 4 V			73	
I_{IH}	Digital high-level input current	V_I = 2.7 V		0	20	μA
I_{IL}	Digital low-level input current	V_I = 0.4 V		−40	−400	μA
I_I	Digital input current	V_I = 7 V			100	μA
I_{refB}	Reference current	V_{refB} = 4 V		−4	−7.2	mA
I_{refT}	Reference current	V_{refT} = 5 V		4	7.2	mA
V_{OH}	High-level output voltage	I_{OH} = −400 μA	2.7			V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA			0.4	V
r_i	Analog input resistance		100			kΩ
C_i	Analog input capacitance			35	65	pF
I_{CC}	Supply current			40	60	mA

operating characteristics over operating supply voltage range, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
E_L	Linearity error				±0.8	%FSR
f_{max}	Maximum conversion rate		20	25		MHz
t_d	Digital output delay time	See Figure 3		15	30	ns

3 Product Previews

timing diagram



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TYPICAL CHARACTERISTICS

IDEAL CONVERSION CHARACTERISTICS

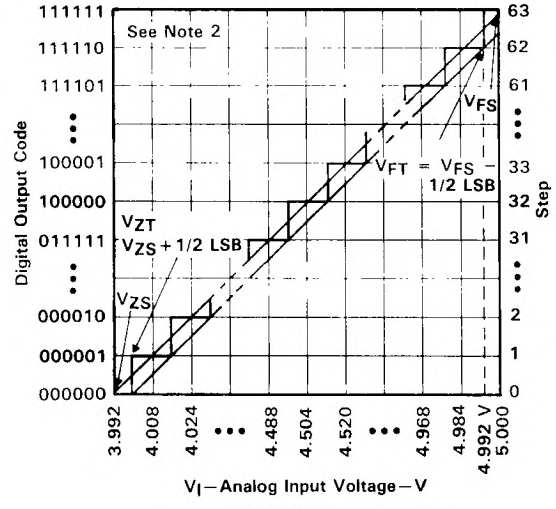


FIGURE 1

END-POINT LINEARITY ERROR

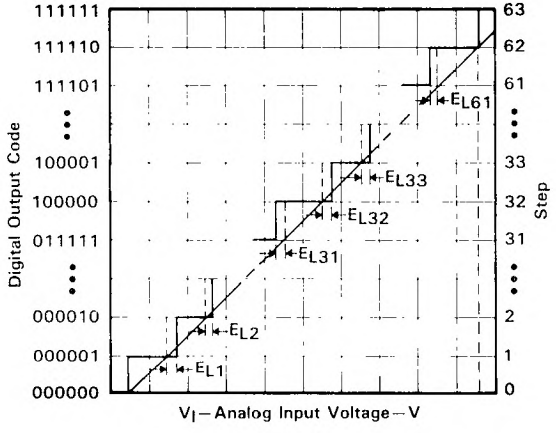


FIGURE 2

NOTE 2: This curve is based on the assumption that V_{refB} and V_{refT} have been adjusted so that the voltage at the transition from digital 0 to 1 (V_{ZT}) is 4.000 V and the transition to full scale (V_{FT}) is 4.992 V. 1 LSB = 16 mV.

3 Product Previews

PARAMETER MEASUREMENT INFORMATION

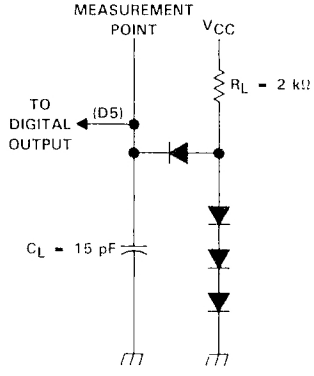


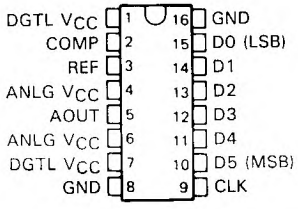
FIGURE 3. LOAD CIRCUIT

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D3154, OCTOBER 1988

- 6-Bit Resolution
- ±0.8% Linearity
- Maximum Conversion Rate . . . 30 MHz Typ
  20 MHz Min
- Analog Output Voltage Range . . . V_{CC} to V_{CC} −1 V
- TTL Digital Input Voltage
- Low Power Consumption . . . 200 mW Typ
- 5-V Single-Supply Operation
- Interchangeable with Fujitsu MB40776

N PACKAGE
(TOP VIEW)

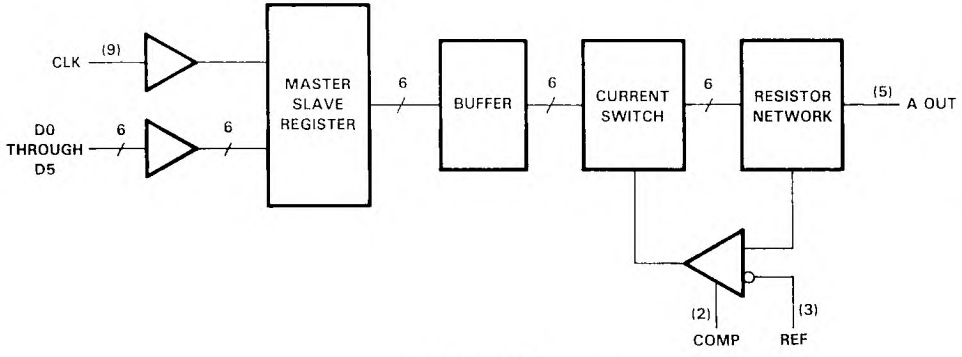


description

The TL5601 is a low-power ultra-high-speed video digital-to-analog converter that uses the Advanced Low-Power Schottky (ALS) process. It converts digital signals to analog signals at a sampling rate of dc to 20 MHz. Because of such high-speed capability, the TL5601 is suitable for digital video applications such as digital television, video processing with a computer, and radar signal processing.

The TL5601C is characterized for operation from 0°C to 70°C.

functional block diagram

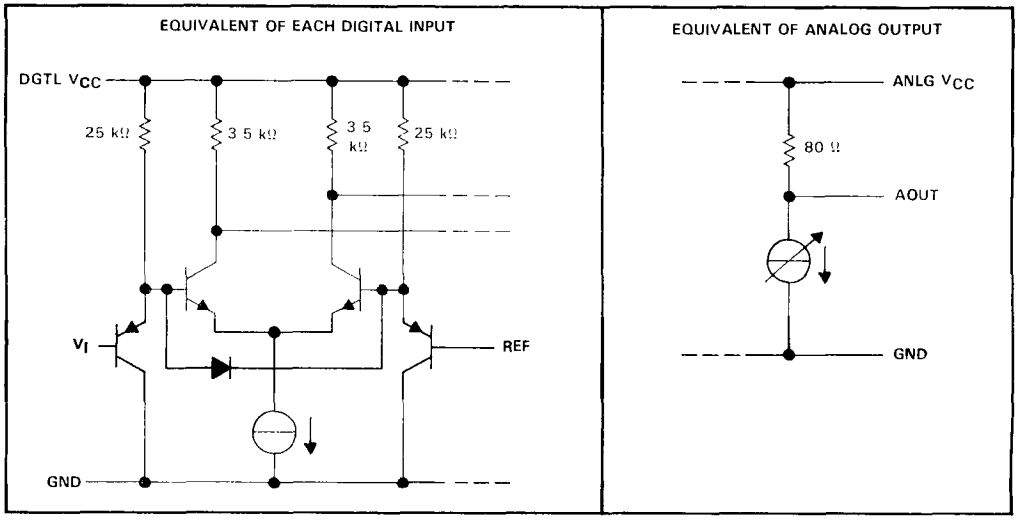


FUNCTION TABLE

STEP	DIGITAL INPUTS						OUTPUT VOLTAGE†
	D5	D4	D3	D2	D1	D0	
0	L	L	L	L	L	L	3.992 V
1	L	L	L	L	L	H	4.008 V
⋮							⋮
31	L	H	H	H	H	H	4.488 V
32	H	L	L	L	L	L	4.504 V
33	H	L	L	L	L	H	4.520 V
⋮							⋮
62	H	H	H	H	H	L	4.984 V
63	H	H	H	H	H	H	5.000 V

†For V_{CC} = 5 V, V_{ref} = 3.976 V

schematics of equivalent input and output circuits



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, ANLG V_{CC}, DGTL V_{CC} . . . . . −0.5 V to 7 V
Digital input voltage range, V_I . . . . . −0.5 V to 7 V
Analog reference voltage range, V_{ref} . . . . . 3.8 V to V_{CC} +0.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{ref}	Analog reference voltage (see Note 1)	3.8	4	4.2	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
t_w	Pulse duration, CLK high or low	25			ns
t_{su}	Setup time, data before CLK↑	12.5			ns
t_h	Hold time, data after CLK↑	12.5			ns
C_{comp}	Phase compensation capacitance (see Note 2)	1			μF
T_A	Operating free-air temperature	0		70	°C

NOTES: 1. V_{ref} must be within 1.2 V of V_{CC}.
2. This capacitor should be connected between comp and GND.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_I	Input current at maximum input voltage	V_I = 7 V		0	100	μA
I_{IH}	High-level input current	V_I = 2.7 V		0	20	μA
I_{IL}	Low-level input current	V_I = 0.4 V		−40	−:	μA
I_{ref}	Input reference current	V_{ref} = 4 V			·0	μA
V_{FS}	Full-scale analog output voltage	V_{CC} = 5 V, V_{ref} = 3.976 V,	V_{CC} − 15	V_{CC}	V_{CC} + 15	mV
V_{ZS}	Zero-scale analog output voltage	I_O = 0 (no load)	3.932	3.992	4.052	V
r_o	Output resistance	T_A = 25°C	70	80	90	Ω
I_{CC}	Supply current	V_{ref} = 4.05 V		48	65	mA

operating characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
E_L	Linearity error				±0.8	%FSR
f_{max}	Maximum conversion rate		20	30		MHz

†All typical values are at V_{CC} = 5 V, V_{ref} = 4 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

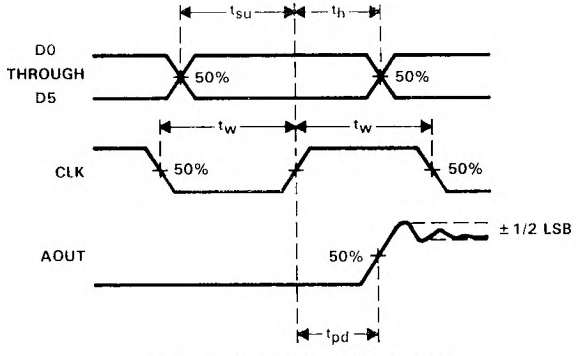


FIGURE 1. VOLTAGE WAVEFORMS

TYPICAL CHARACTERISTICS

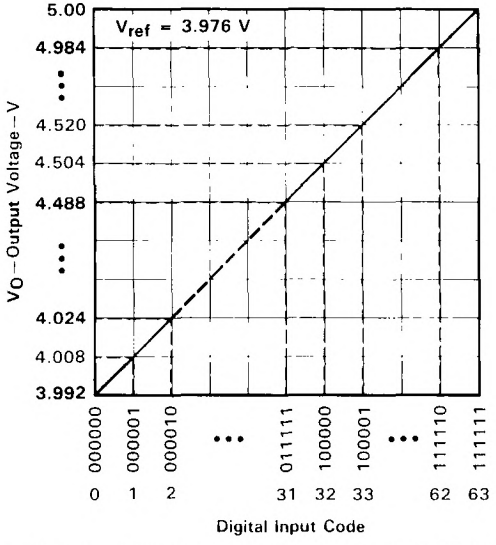


FIGURE 2. IDEAL CONVERSION CHARACTERISTICS

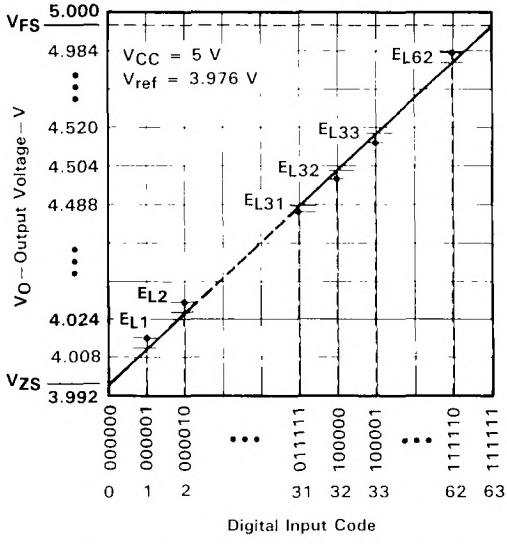


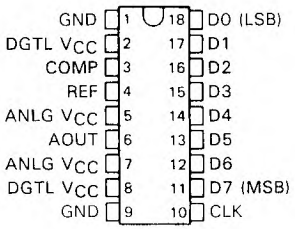
FIGURE 3. END-POINT LINEARITY ERROR

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D3094, SEPTEMBER 1988

- 8-Bit Resolution
- ±0.2% Linearity
- Maximum Conversion Rate . . . 30 MHz Typ
  20 MHz Min
- Analog Output Voltage Range . . . V_{CC} to V_{CC} – 1 V
- TTL Digital Input Voltage
- 5-V Single-Supply Operation
- Low Power Consumption . . . 250 mW Typ
- Interchangeable with Fujitsu MB40778

N PACKAGE
(TOP VIEW)

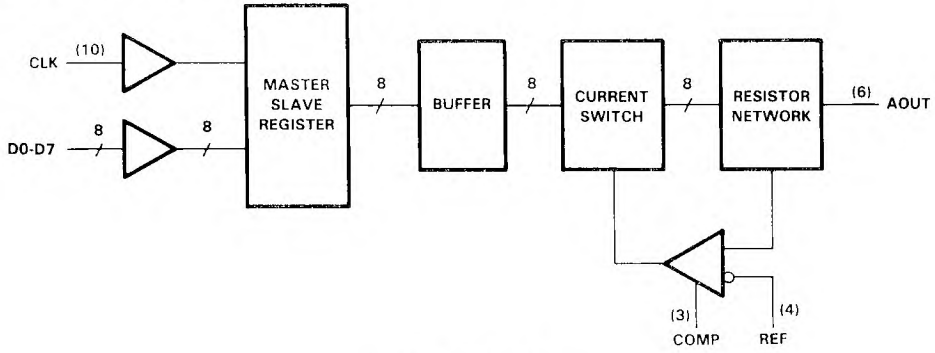


description

The TL5602 is a low-power ultra-high-speed video digital-to-analog converter that uses the Advanced Low-Power Schottky (ALS) process. It converts digital signals to analog signals at a sampling rate of dc to 20 MHz. Because of such high-speed capability, the TL5602 is suitable for digital video applications such as digital television, video processing with a computer, and radar signal processing.

The TL5602C is characterized for operation from 0°C to 70°C.

functional block diagram



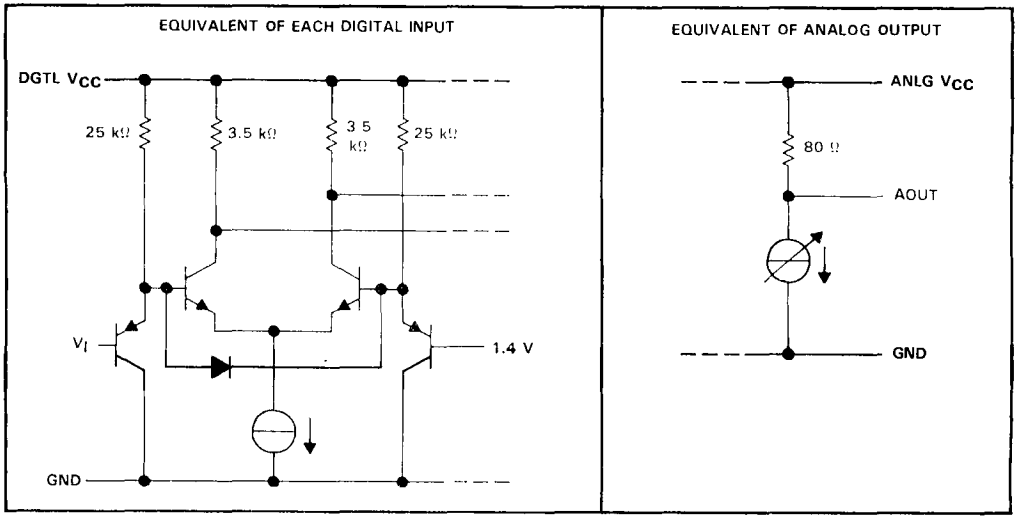
FUNCTION TABLE

STEP	DIGITAL INPUTS								OUTPUT VOLTAGE†
	D7	D6	D5	D4	D3	D2	D1	D0	
0	L	L	L	L	L	L	L	L	3.980 V
1	L	L	L	L	L	L	L	L	3.984 V
⋮					⋮				⋮
127	L	H	H	H	H	H	H	H	4.488 V
128	H	L	L	L	L	L	L	L	4.492 V
129	H	L	L	L	L	L	L	H	4.496 V
⋮					⋮				⋮
254	H	H	H	H	H	H	H	L	4.996 V
255	H	H	H	H	H	H	H	H	5.000 V

†For V_{CC} = 5 V, V_{ref} = 3.976 V

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

schematics of equivalent input and output circuits



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, ANLG V_{CC}, DGTL V_{CC} . . . . . −0.5 V to 7 V
Digital input voltage range, V_I . . . . . −0.5 V to 7 V
Analog reference voltage range, V_{ref} . . . . . 3.8 V to V_{CC} +0.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{ref}	Analog reference voltage (see Note 1)	3.8	4	4.2	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
t_w	Pulse duration, CLK high or low	25			ns
t_{su}	Setup time, data before CLK↑	12.5			ns
t_h	Hold time, data after CLK↑	12.5			ns
C_{comp}	Phase compensation capacitance (see Note 2)	1			μF
T_A	Operating free-air temperature	0		70	°C

NOTES: 1. $V_{CC} - V_{ref} \leq 1.2$ V
2. This capacitor should be connected between COMP and GND

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_I	Input current at maximum input voltage	V_{CC} = 5.25 V, V_I = 7 V		0	100	μA
I_{IH}	High-level input current	V_{CC} = 5.25 V, V_I = 2.7 V		0	20	μA
I_{IL}	Low-level input current	V_{CC} = 5.25 V, V_I = 0.4 V		−40	−400	μA
I_{ref}	Input reference current	V_{ref} = 4 V			10	μA
V_{FS}	Full-scale analog output voltage	V_{CC} = 5 V, V_{ref} = 3.976 V,	V_{CC}−15		V_{CC}+15	mV
V_{ZS}	Zero-scale analog output voltage	I_O = 0 (no load)	3.919	[illegible]	4.042	V
r_o	Output resistance	T_A = 25°C	70	80	90	Ω
I_{CC}	Supply current	V_{ref} = 4.05 V		50	75	mA

†All typical values are at V_{CC} = 5 V, V_{ref} = 4 V, T_A = 25°C

operating characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
E_L	Linearity error				±0.2	%FSR
f_{max}	Maximum conversion rate		20	30		MHz

3

Product Previews

PARAMETER MEASUREMENT INFORMATION

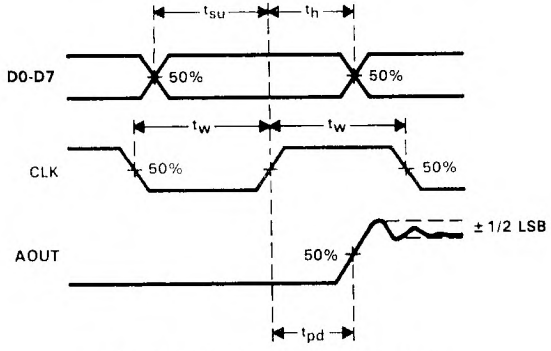


FIGURE 1. VOLTAGE WAVEFORMS

TYPICAL CHARACTERISTICS

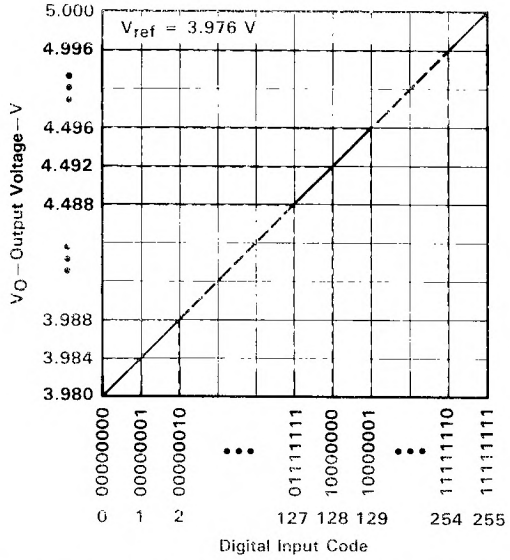


FIGURE 2. IDEAL CONVERSION CHARACTERISTICS

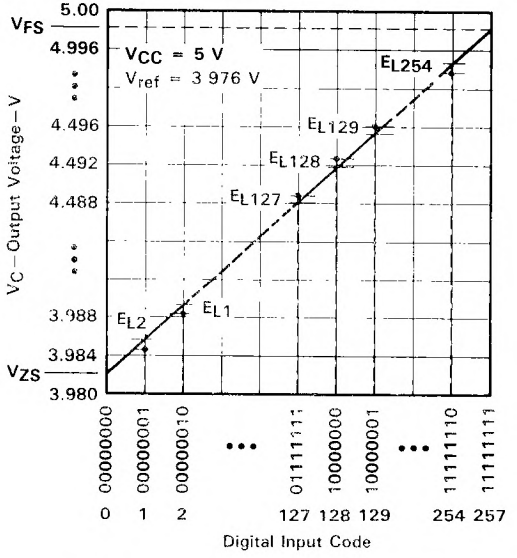
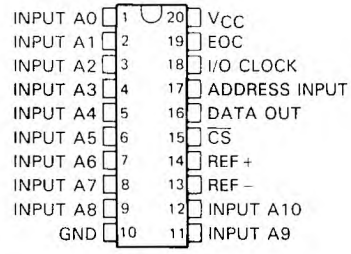


FIGURE 3. END-POINT LINEARITY ERROR

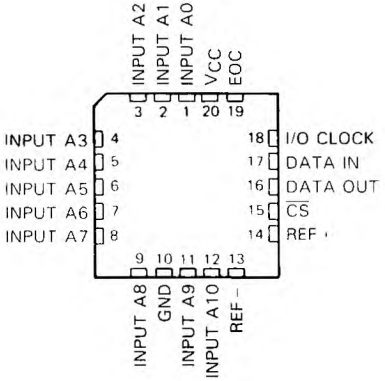
TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

- LinCMOS™ Technology
- 8-Bit Resolution A/D Converter
- Microprocessor Peripheral or Stand-Alone Operation
- On-Chip 12-Channel Analog Multiplexer
- Built-In Self-Test Mode
- Software-Controllable Sample and Hold
- Total Unadjusted Error . . . ±0.5 LSB Max
- Direct Replacement for Motorola MC145041
- On-Board System Clock
- End-Of-Conversion (EOC) Output
- Pinout and Control Signals Compatible with TLC540 and TLC1540 Family of 10-Bit A/D Converters

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



TYPICAL PERFORMANCE

Channel Acquisition/Sample Time	1.6 µs
Conversion Time	20 µs
Samples per Second	25×10^3
Power Dissipation	10 mW

description

The TLC542 is a LinCMOS™ A/D peripheral built around an 8-bit switched-capacitor successive-approximation A/D converter. The device is designed for serial interface to a microprocessor or peripheral via a 3-state output with three inputs (including I/O Clock, Chip Select ($\overline{CS}$), and Address Input). The TLC542 allows high-speed data transfers and sample rates of up to 40,000 samples per second. In addition to the high-speed converter and versatile control logic, an on-chip 12-channel analog multiplexer can sample any one of 11 inputs or an internal "self-test" voltage, and the sample-and-hold is started under microprocessor control. At the end of conversion, the End-Of-Conversion (EOC) output pin goes high to indicate that conversion is complete. Detailed information on interfacing to most popular microprocessors is readily available from the factory.

The converter incorporated in the TLC542 features differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and isolation of analog circuitry from logic and supply noises. A switched-capacitor design allows low-error (±0.5 LSB) conversion in 20 µs over the full operating temperature range.

The TLC542 is available in both the N and FN plastic packages. The TLC542M is characterized for operation from −55°C to 125°C, and the TLC542I is characterized for operation from −40°C to 85°C.

LinCMOS is a trademark of Texas Instruments Incorporated.

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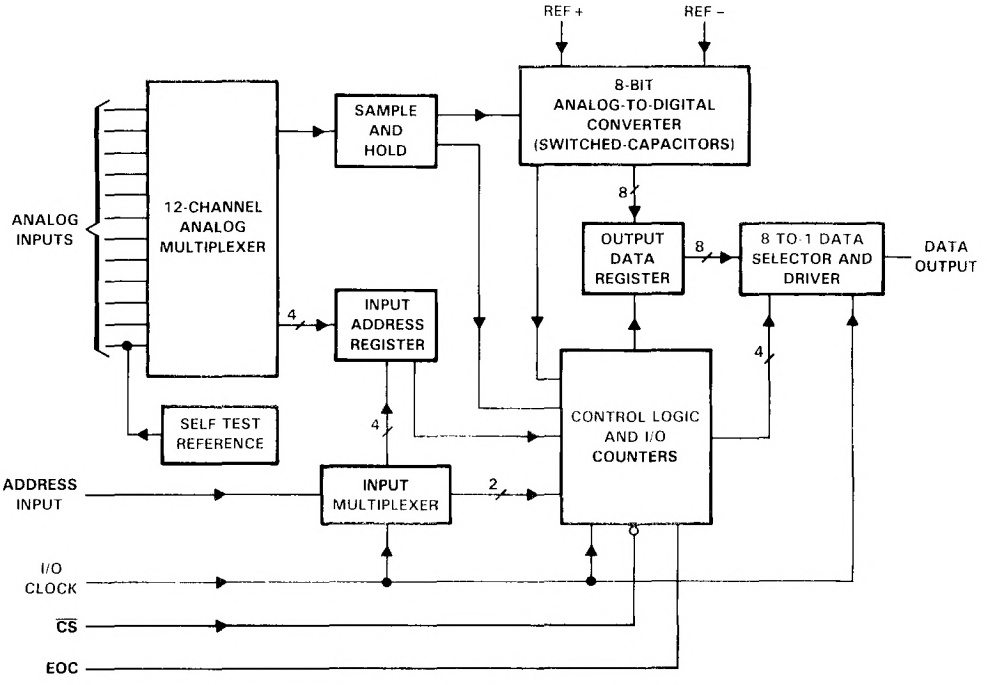
functional block diagram



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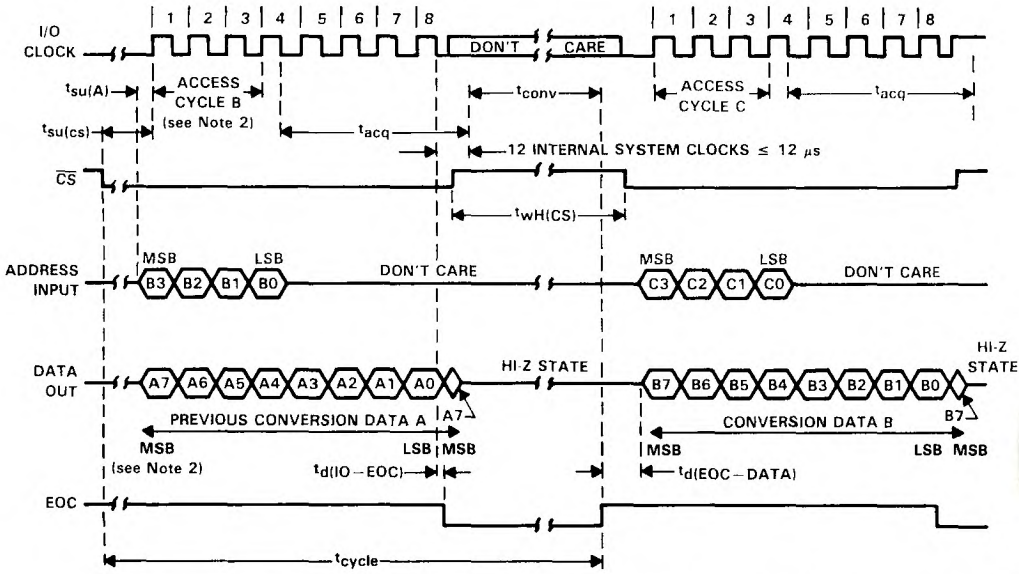
operating sequence



NOTES: 1. The conversion cycle, which requires 36 internal system clock periods, is initiated on the 8th falling edge of the I/O Clock after $\overline{CS}$ goes low for the channel whose address exists in memory at that time. If $\overline{CS}$ is kept low during conversion, the I/O Clock must remain low for at least 36 system clock cycles to allow conversion to be completed.

2. To minimize errors caused by noise at the chip select input, the internal circuitry waits for two rising edges and one falling edge of the internal system clock after $\overline{CS}$ ↓ before responding to control input signals. The $\overline{CS}$ setup time is given by the $t_{su(CS)}$ specifications. Therefore, no attempt should be made to clock-in an address until the minimum chip select setup time has elapsed.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 3) . . . . . 6.5 V
Input voltage range (any input) . . . . . −0.3 V to V_{CC} +0.3 V
Output voltage range . . . . . −0.3 V to V_{CC} +0.3 V
Peak input current range (any input) . . . . . ±20 mA
Peak total input current (all inputs) . . . . . ±30 mA
Operating free-air temperature: TLC542M . . . . . −55°C to 125°C
TLC542I . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

NOTE 3: All voltage values are with respect to digital ground with REF− and GND wired together (unless otherwise noted)

recommended operating conditions, V_{CC} = 4.75 V to 5.5 V

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.5	V
Positive reference voltage, V_{REF+} (see Note 4)		2.5	V_{CC}	V_{CC} + 0.1	V
Negative reference voltage, V_{REF-} (see Note 4)		0.1	0	2.5	V
Differential reference voltage, $V_{REF+} - V_{REF-}$ (see Note 4)		1	V_{CC}	V_{CC} + 0.2	V
Analog input voltage (see Note 4)		0		V_{CC}	V
High-level control input voltage, V_{IH}		2			V
Low-level control input voltage, V_{IL}				0.8	V
Setup time, address bits at data input before I/O CLK ↑, $t_{su(A)}$		400			ns
Hold time, address bits after I/O CLK ↑, $t_{h(A)}$		0			ns
Hold time, $\overline{CS}$ low after 8th I/O CLK ↓, $t_{h(CS)}$		0			ns
Setup time, $\overline{CS}$ low before clocking in first address bit, $t_{su(CS)}$ (see Note 2)		1.4			µs
$\overline{CS}$ high during conversion, $t_{wH(CS)}$		17			µs
Input/Output clock frequency, $f_{CLK(I/O)}$		0		1.1	MHz
Input/Output clock high, $t_{wH(I/O)}$		404			ns
Input/Output clock low, $t_{wL(I/O)}$		404			ns
I/O Clock transition time (see Note 5)	$f_{CLK(I/O)}$ ≤ 525 kHz			100	ns
	$f_{CLK(I/O)}$ > 525 kHz			40	
Operating free-air temperature, T_A	TLC542M	−55		125	°C
	TLC542I	−40		85	

NOTES: 2. To minimize errors caused by noise at the chip select input, the internal circuitry waits for two rising edges and one falling edge of the internal system clock after $\overline{CS}$ ↓ before responding to control input signals. The $\overline{CS}$ setup time is given by the $t_{su(CS)}$ specifications. Therefore, no attempt should be made to clock-in an address until the minimum chip select setup time has elapsed.

4. Analog input voltages greater than that applied to REF+ convert as all ones (11111111), while input voltages less than that applied to REF− convert as all zeros (00000000). For proper operation, REF+ must be at least 1 V higher than REF−. Also, the total unadjusted error may increase as this differential reference voltage falls below 4 75 V.

5. This is the time required for the clock input signal to fall from V_{IH} min to V_{IL} max or to rise from V_{IL} max to V_{IH} min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 2 µs for remote data acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics over recommended operating temperature range, $V_{CC} = V_{REF+} = 4.75$ V to 5.5 V (unless otherwise noted), $f_{CLK(I/O)} = 1.1$ MHz

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage (pin 16)		V_{CC} = 4.75 V, I_{OH} = −360 µA		2.4			V
V_{OL}	Low-level output voltage		V_{CC} = 4.75 V, I_{OL} = 1.6 mA				0.4	V
I_{OZ}	Off-state (high-impedance state) output current		$V_O = V_{CC}$, $\overline{CS}$ at V_{CC}				10	µA
			V_O = 0, $\overline{CS}$ at V_{CC}				−10	
I_{IH}	High-level input current		$V_I = V_{CC}$			0.005	2	µA
I_{IL}	Low-level input current		V_I = 0			−0.005	−2.5	µA
I_{CC}	Operating supply current		$\overline{CS}$ at 0 V			1.2	2	mA
	Selected channel leakage current		Selected channel at V_{CC},	−55°C to 125°C			1	µA
			Unselected channel at 0 V	−40°C to 85°C			0.4	
			Selected channel at 0 V,	−55°C to 125°C			−1	
			Unselected channel at V_{CC}	−40°C to 85°C			−0.4	
I_{REF}	Maximum s current into	analog reference +	$V_{REF+} = V_{CC}$, V_{REF-} = GND				10	µA
C_i	Input capacitance	Analog inputs				7	55	pF
		Control inputs				5	15	

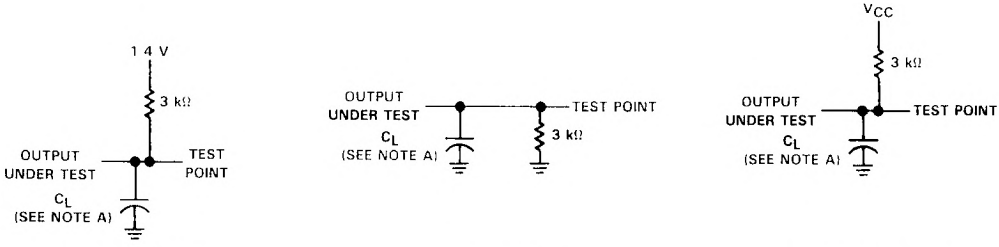
† All typical values are at T_A = 25°C.

operating characteristics over recommended operating free-air temperature range, $V_{CC} = V_{REF+} = 4.75$ V to 5.5 V, $f_{CLK(I/O)} = 1$ MHz

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Linearity error (see Note 7)				±0.5	LSB
	Zero error (see Note 8)	See Note 6			±0.5	LSB
	Full-scale error (see Note 8)	See Note 6			±0.5	LSB
	Total unadjusted error (see Note 9)				±0.5	LSB
	Self-test output code	Input A11 address = 1011, See Note 10	01111101 (125)		10000011 (131)	
t_{conv}	Conversion time	See operating sequence			20	µs
t_{cycle}	Total access and conversion cycle time	See operating sequence			40	µs
t_{acq}	Channel acquisition time (sample cycle)	See operating sequence			16	µs
t_v	Time output data remains valid after I/O CLK ↓	See Figure 5	10			ns
$t_{d(IO-DATA)}$	Delay time, I/O CLK ↓ to data output valid	See Figure 5			400	ns
$t_{d(IO-EOC)}$	Delay time, 8th I/O CLK ↓ to EOC ↓	See Figure 6			500	ns
$t_{d(EOC-DATA)}$	Delay time, EOC ↑ to data out (MSB)	See Figure 7			400	ns
t_{PZH}, t_{PZL}	Delay time, $\overline{CS}$ ↓ to data out (MSB)	See Figure 2			3.4	µs
t_{PHZ}, t_{PLZ}	Delay time, $\overline{CS}$ ↑ to data out	See Figure 2			150	ns
$t_{r(EOC)}$	Rise time	See Figure 7			100	ns
$t_{f(EOC)}$	Fall time	See Figure 6			100	ns
$t_{r(bus)}$	Data bus rise time	See Figure 5			300	ns
$t_{f(bus)}$	Data bus fall time	See Figure 5			300	ns

NOTES: 6. Analog input voltages greater than that applied to REF+ convert to all ones (11111111), while input voltages less than that applied to REF− convert to all zeros (00000000). For proper operation, REF+ must be at least 1 V higher than REF−. Also, the total unadjusted error may increase as this differential reference voltage falls below 4.75 V.
7. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
8. Zero error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted output for full-scale input voltage.
9. Total unadjusted error is the sum of linearity, zero, and full-scale errors.
10. Both the input address and the output codes are expressed in positive logic. The A11 analog input signal is internally generated and is used for test purposes.

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L = 50 pF

FIGURE 1. LOAD CIRCUITS

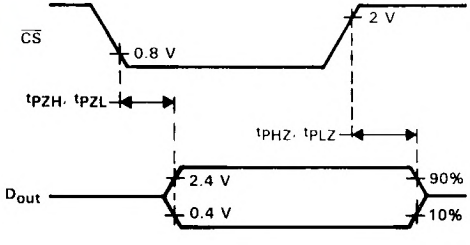


FIGURE 2

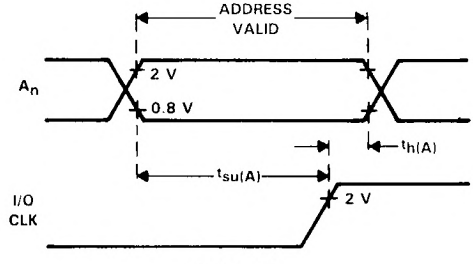


FIGURE 3

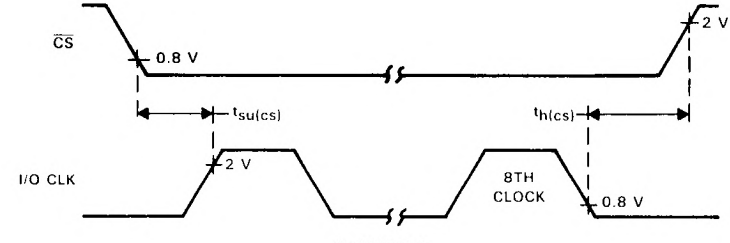


FIGURE 4

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PARAMETER MEASUREMENT INFORMATION

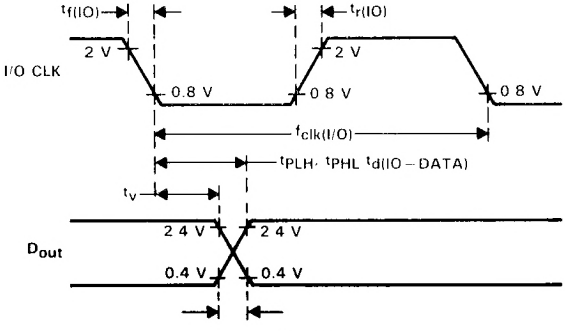

FIGURE 5

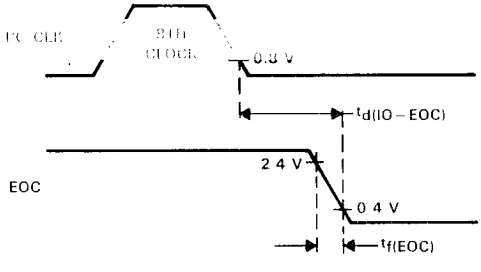

FIGURE 6

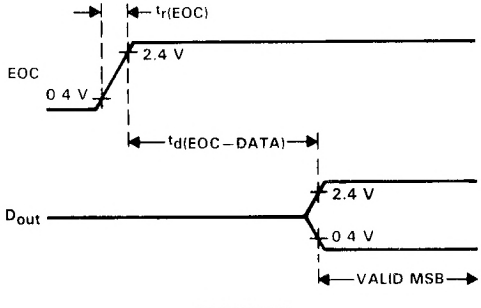

FIGURE 7

principles of operation

The TLC542 is a complete data acquisition system on a single chip. The device includes such functions as analog multiplexer, sample-and-hold, 8-bit A/D converter, data and control registers, and control logic. Three control inputs (I/O clock, chip select ($\overline{CS}$), and address) are included for flexibility and access speed. These control inputs and a TTL-compatible 3-state output are intended for serial communications with a microprocessor or microcomputer. With judicious interface timing, the TLC542 can complete a conversion in 20 μs, while complete input-conversion-output cycles can be repeated every 40 μs. Furthermore, this fast conversion can be executed on any of 11 inputs or its built-in "self-test" and in any order desired by the controlling processor.

When $\overline{CS}$ is high, the Data Output pin is in a 3-state condition and the Address Input and I/O Clock pins are disabled. When additional TLC542 devices are used, this feature allows each of these pins, with the exception of the $\overline{CS}$ pin, to share a control logic point with their counterpart pins on additional A/D devices. Thus, this feature minimizes the control logic pins required when using multiple A/D devices.

The control sequence is designed to minimize the time and effort required to initiate conversion and to obtain the conversion result. A normal control sequence is as follows:

1. $\overline{CS}$ is brought low. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for two rising edges and then a falling edge of the internal system clock before recognizing the low $\overline{CS}$ transition. The MSB of the result of the previous conversion automatically appears on the Data Out pin.
2. On the first four rising edges of the I/O Clock, a new positive-logic multiplexer address is shifted in, with the MSB of this address shifted first. The negative edges of these four I/O clock pulses shift out the second, third, fourth, and fifth most significant bits of the result of the previous conversion. The on-chip sample-and-hold begins sampling the newly addressed analog input after the fourth falling edge of the I/O Clock. The sampling operation basically involves charging the internal capacitors to the level of the analog input voltage.
3. Three clock cycles are applied to the I/O pin, and the sixth, seventh, and eighth conversion bits are shifted out on the negative edges of these clock cycles.
4. The final eighth clock cycle is applied to the I/O Clock pin. The falling edge of this clock cycle completes the analog sampling process and initiates the hold function. Conversion is then performed during the next 20 μs. After this final I/O Clock cycle, $\overline{CS}$ must go high or the I/O Clock must remain low for at least 20 μs to allow for the conversion function.

$\overline{CS}$ can be kept low during periods of multiple conversion. If $\overline{CS}$ is taken high, it must remain high until the end of the conversion. Otherwise, a valid falling edge of $\overline{CS}$ causes a reset condition, which aborts the conversion process.

A new conversion may be started and the ongoing conversion simultaneously aborted by performing steps 1 through 4 before the 20-μs conversion time has elapsed. Such action yields the conversion result of the previous conversion and not the ongoing conversion.

The End-Of-Conversion (EOC) output goes low on the negative edge of the eighth I/O Clock. The subsequent low-to-high transition of EOC indicates the A/D conversion is complete and the conversion result is ready for transfer.

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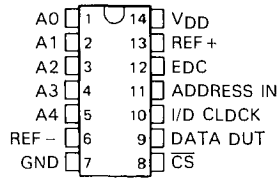
D2799, SEPTEMBER 1986

- LinCMOS™ Technology
- 8-Bit Resolution A/D Converter
- On-Chip 6-Channel Analog Multiplexer
- Built-In Self-Test Mode
- Software-Controllable Sample-and-Hold
- Total Unadjusted Error . . . ±0.5 LSB Max
- End-of-Conversion Output
- Conversion Time . . . 17 μs Max
- Internal System Clock . . . 4 MHz Typ
- Low Power Consumption . . . 6 mW Typ
- Minimum Sample Rates:
  TLC543 . . . 45,500 c/s
  TLC544 . . . 40,000 c/s

D, J, OR N PACKAGE
(TOP VIEW)



description

The TLC543 and TLC544 are LinCMOS™ A/D peripherals built around an 8-bit switched-capacitor, successive-approximation A/D converter. They are designed for serial interface to a microprocessor or peripheral via a 3-state output with up to four control lines including I/O Clock, Chip Select ($\overline{CS}$), Address Input, and End-of-Conversion (EOC) output. A 4-MHz on-chip system clock and simultaneous read/write operations permit high-speed data transfer and minimum sample rates of 45,500 cycles per second for the TLC543 and 40,000 cycles per second for the TLC544. In addition to the high-speed converter and versatile control logic, an on-chip 6-channel analog multiplexer can be used to sample any one of five inputs or an internal "self-test" voltage, and a sample-and-hold can operate automatically or under processor control.

The converters incorporated in the TLC543 and TLC544 feature differential high-impedance reference inputs that permit ratiometric conversion, scaling, and isolation of analog circuitry from logic and supply noise.

A totally switched-capacitor design allows low-error (±0.5 LSB) conversion in 17 microseconds maximum for the TLC543 and the TLC544 over the full operating temperature range. The TLC543M and TLC544M are characterized for operation over the full military temperature range of −55°C to 125°C. The TLC543I and TLC544I are characterized for operation from −40°C to 85°C.

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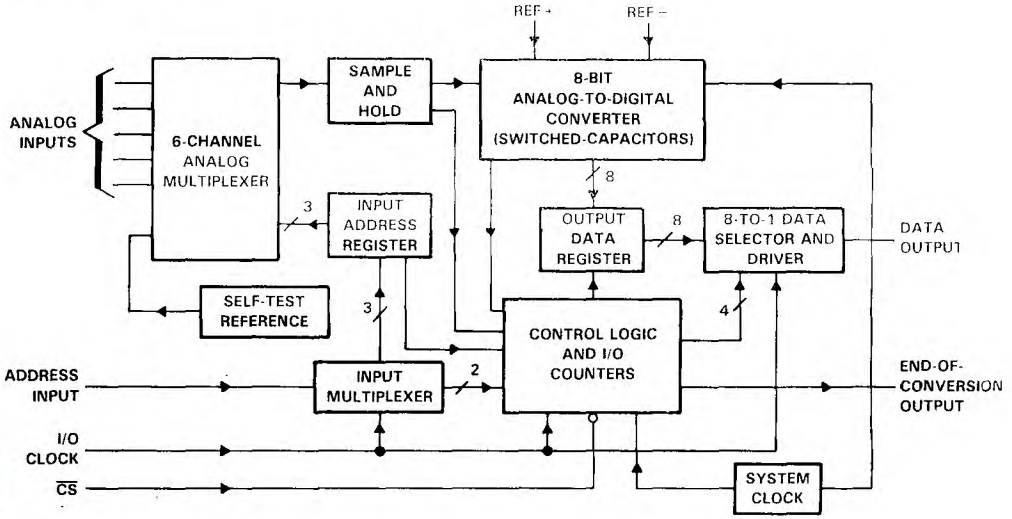
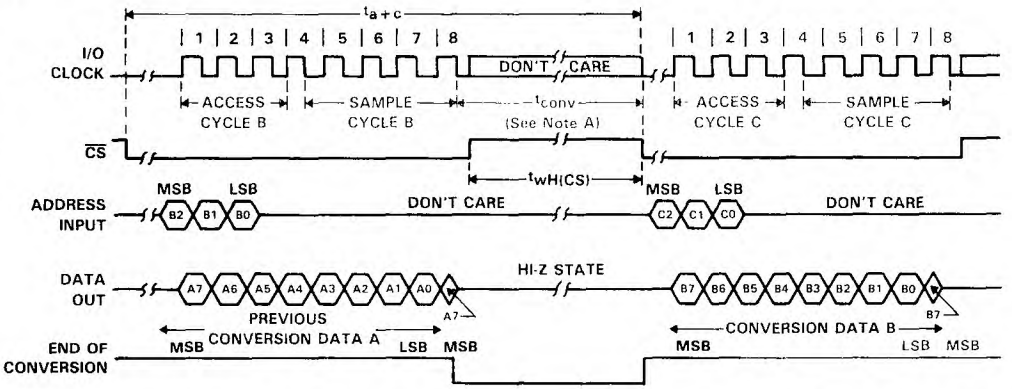
functional block diagram



operating sequence



NOTES: A. The conversion cycle, which requires 36 internal system clock periods, is initiated on the 8th falling edge of the I/O Clock after $\overline{CS}$ goes low for the channel whose address exists in memory at that time. If $\overline{CS}$ is kept low during conversion, the I/O clock must remain low for at least 36 system clock cycles to allow conversion to complete.

B. The most significant bit (MSB) is automatically placed on the DATA OUT bus after $\overline{CS}$ is brought low. The remaining seven bits (A6-A0) are clocked out on the first seven falling edges of the I/O Clock.

C. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for three internal system clock cycles (1.4 μs at 2 MHz) after a chip select transition before responding to control input signals. Therefore, no attempt should be made to clock-in address data until the minimum chip-select setup time has elapsed.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 6.5 V
Input voltage range (any input) . . . . . −0.3 V to V_{CC} + 0.3 V
Output voltage range . . . . . −0.3 V to V_{CC} + 0.3 V
Peak input current (any input) . . . . . ±10 mA
Peak total input current (all inputs) . . . . . ±30 mA
Operating free-air temperature range: TLC543M, TLC544M . . . . . −55°C to 125°C
TLC543I, TLC544I . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTE 1: All voltages are with respect to ground (GND pin) with REF− and GND wired together (unless otherwise noted).

recommended operating conditions

		TLC543			TLC544			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		3	5	6	3	5	6	V
Positive reference voltage, V_{REF+} (see Note 2)		2.5	V_{CC}	V_{CC}+0.1	2.5	V_{CC}	V_{CC}+0.1	V
Negative reference voltage, V_{REF-} (see Note 2)		−0.1	0	2.5	0.1	0	2.5	V
Differential reference voltage, $V_{REF+} - V_{REF-}$ (see Note 2)		1	V_{CC}	V_{CC}+0.2	1	V_{CC}	V_{CC}+0.2	V
Analog input voltage (see Note 2)		0		V_{CC}	0		V_{CC}	V
High-level control input voltage, V_{IH} (for V_{CC} = 4.75 to 5.5 V)		2			2			V
Low-level control input voltage, V_{IL} (for V_{CC} = 4.75 to 5.5 V)				0.8			0 8	V
Input/Output clock frequency, $f_{CLK(I/O)}$ (for V_{CC} = 4.75 to 5.5 V)		0		2.048	0		1.1	MHz
System clock frequency, $f_{CLK(I/O)}$ (for V_{CC} = 4.75 to 5.5 V)				4			2.1	MHz
Input/Output clock high, $t_{wH(I/O)}$		200			404			ns
Input/Output clock low, $t_{wL(I/O)}$		200			404			ns
I/O clock transition time (see Note 3)	$f_{CLK(I/O)}$ < 1.1 MHz			100			100	ns
	$f_{CLK(I/O)}$ > 1.1 MHz			40				
Duration of $\overline{CS}$ input high state during conversion, $t_{wH(CS)}$		17			17			µs
Setup time, address bits at data input before I/O CLOCK↑, $t_{su(A)}$		200			400			ns
Hold time, address bits after I/O CLOCK↑, $t_{h(A)}$		0			0			ns
Setup time, $\overline{CS}$ low before clocking in first address bits, $t_{su(CS)}$ (see Note 4)		1.4			1.4			µs
Operating free-air temperature, T_A	TLC543M, TLC544M	−55		125	−55		125	°C
	TLC543I, TLC544I	−40		85	−40		85	

NOTES: 2. Analog input voltages greater than that applied to REF+ convert to all ones (11111111), and input voltages less than that applied to REF− convert to all zeros (00000000). For proper operation, REF+ voltage must be at least 1 V higher than REF− voltage. Also, adjusted errors may increase as this differential reference voltage falls below 4.75 V.

3. This is the time required for the clock input signal to fall from V_{IH} min to V_{IL} max or to rise from V_{IL} max to V_{IH} min. In the vicinity of normal room temperature, the devices function with input clock transitions as slow as 2 µs for remote data acquisition applications in which the sensor and the A/D converter are placed several feet away from the controlling microprocessor.

4. To minimize errors caused by noise at the Chip Select input, the internal circuitry waits for three system clock cycles (1.4 µs at 2 MHz) after a chip select falling edge is detected before responding to control input signals. Therefore, no attempt should be made to clock-in address data until the minimum chip select setup time has elapsed.

electrical characteristics over recommended operating temperature range, $V_{CC} = V_{REF+} = 4.75$ V to 5.5 V (unless otherwise noted), $f_{CLK(I/O)} = 2.048$ MHz for TLC543 or $f_{CLK(I/O)} = 1.1$ MHz for TLC544

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage, Data out, EOC		V_{CC} = 4.75 V,	I_{OH} = −360 μA	2.4			V
V_{OL}	Low-level output voltage	Data out	V_{CC} = 4.75 V,	I_{OL} = 3.2 mA			0.4	V
			V_{CC} = 4.75 V,	I_{OL} = 1.6 mA			0.4	
I_{OZ}	Off-state (high-impedance state) output current		$V_O = V_{CC}$,	$\overline{CS}$ at V_{CC}			10	μA
			V_O = 0,	$\overline{CS}$ at V_{CC}			−10	
I_{IH}	High-level input current		$V_I = V_{CC}$ + 0.3 V			0.005	2.5	μA
I_{IL}	Low-level input current		V_I = 0			−0.005	−2.5	μA
I_{CC}	Operating supply current		$\overline{CS}$ at 0 V			1.2	2	mA
I_{lkg}	Selected channel leakage current		Selected channel at V_{CC}, Unselected channel at 0 V	See Figure 1		0.4	1	μA
			Selected channel at 0 V, Unselected channel at V_{CC}			−0.4	−1	
I_{REF}	Reference current		$V_{REF+} = V_{CC}$,	$\overline{CS}$ at 0 V		0.1	1	mA
C_i	Input capacitance	Analog inputs				7	55	pF
		Control inputs				5	15	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

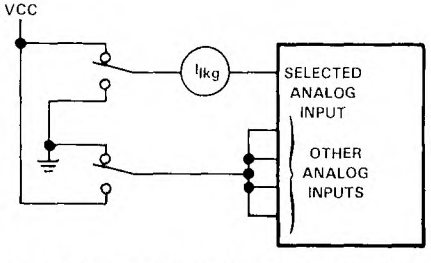

FIGURE 1. SELECTED CHANNEL LEAKAGE CURRENT

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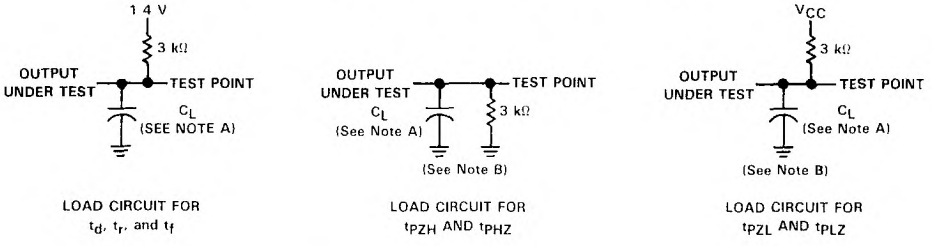
operating characteristics over recommended operating free-air temperature range, V_{CC} = V_{REF+} = 4.75 to 5.5 V, $f_{CLK(I/O)}$ = 2.048 MHz for TLC543 or 1.1 MHz for TLC544

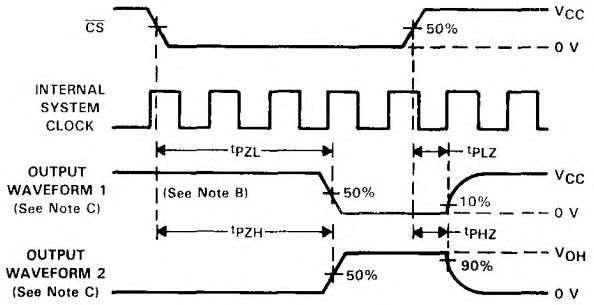
PARAMETER		TEST CONDITIONS	TLC543			TLC544			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
	Linearity error (see Note 5)				±0.5			±0.5	LSB
	Zero error (see Note 6)				±0.5			±0.5	LSB
	Full-scale error (see Note 6)				±0.5			±0.5	LSB
	Total unadjusted error (see Note 7)				±0.5			±0.5	LSB
	Self-test output code	Input A5 address = 101_{10}, See Note 8	01111101 (125)		10000011 (131)	01111101 (125)		10000011 (131)	
t_{conv}	Conversion time	See Operating Sequence		13	17		12	17	µs
t_{a+c}	Total access and conversion time	See Operating Sequence		12	22		19	25	µs
t_{acq}	Channel acquisition time (sample cycle)	See Operating Sequence			4			4	I/O clock cycles
t_v	Time output data remains valid after I/O clock↓		10			10			ns
t_d	Delay time, I/O clock↓ to data output valid				300			400	ns
t_{en}	Output enable time	See Figure 2			1.4			1.4	ns
t_{dis}	Output disable time				150			150	ns
$t_{r(bus)}$	Data bus and CS rise time				300			300	ns
$t_{f(bus)}$	Data bus and CS fall time				300			300	ns
$t_{PHL(EOC)}$	Propagation delay, 8th I/O clock↓ to EOC				400			400	ns
$t_{d(EOC)}$	Delay time, EOC to DATA OUT (MSB) (see Note 9)			1			−1		µs

NOTES: 5. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
6. Zero error is the difference between the output of an ideal and an actual A/D converter for zero input voltage; full-scale error is that same difference for full-scale input voltage.
7. Total unadjusted error comprises linearity, zero, and full-scale errors
8. Both the input address and the output codes are expressed in positive logic. The A5 analog input signal is internally generated and is used for test purposes.
9. *The EOC signal is output after 40 internal clock cycles, while the data is available after 36 internal clock cycles. Thus, the delay time, EOC to DATA OUT,* is a negative value equal to four internal system clock cycles less internal propagation delay.

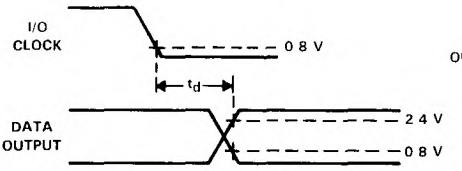
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR t_d, t_r, and t_f | LOAD CIRCUIT FOR t_{PZH} AND t_{PHZ} | LOAD CIRCUIT FOR t_{PZL} AND t_{PLZ}

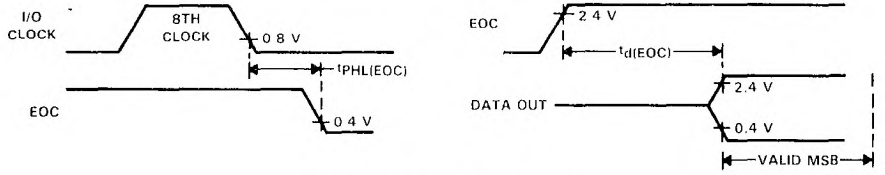


VOLTAGE WAVEFORMS FOR ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORM FOR DELAY TIME

VOLTAGE WAVEFORM FOR RISE AND FALL TIMES



VOLTAGE WAVEFORMS FOR EOC TIMING

NOTES: A. C_L = 50 pF for TLC543 and 100 pF for TLC544
B. t_{en} = t_{PZH} or t_{PZL}, t_{dis} = t_{PHZ} or t_{PLZ}
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

FIGURE 2. OPERATING CHARACTERISTICS

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PRINCIPLES OF OPERATION

introduction

TLC543 and TLC544 are each complete data acquisition systems on a single chip. They include the functions of analog multiplexer, sample-and-hold, 8-bit A/D converter, data and control registers, and control logic. Flexible serial communication is achieved with a microprocessor or microcomputer using a TTL-compatible 3-state Data Out and four control lines — Chip Select ($\overline{CS}$), I/O Clock, Address Input, and End of Conversion (EOC) output.

To maximize access speed, the device simultaneously writes the previous conversion result, reads a new multiplexer address, and acquires the analog signal. This is followed by the A/D conversion, whose end is signalled by the EOC output going high. These total access and conversion cycles are completed in a minimum of 22 μs for the TLC543 and 25 μs for the TLC544. Conversion can take place, in any order, on the five analog inputs or the built-in self-test system.

The system clock, which drives the control logic and the switched-capacitor successive-approximation A/D converter, is internal to the device and typically runs at a frequency of 4 MHz. This internal system clock runs independently, and there are no required phase or frequency relationships with other signals.

digital interface

The I/O clock controls the acquisition of the analog signal as well as all serial data communications between the TLC543 or TLC544 and the host processor. From the host, this I/O clock consists of a burst of eight pulses separated by the conversion time. Timing may be achieved by Chip Select ($\overline{CS}$) synchronously gating a continuous I/O clock or directly from the host with $\overline{CS}$ held low continuously.

With $\overline{CS}$ high, Data Out is in a high-impedance condition with the Address Input and I/O Clock input disabled. This feature allows the interface pins, with the exception of $\overline{CS}$ and EOC, to share a common bus with additional TLC543 or TLC544 devices or other members of the TLC543/544 family of devices.

typical operating sequence

Consider an access and conversion sequence where $\overline{CS}$ is being used: $\overline{CS}$ is brought low and recognized after the time out of the noise-rejection circuitry. The MSB of the result of the previous conversion appears at Data Out, whose 3-state output is enabled. The MSB of the new multiplexer address should be present at the Address Input to conform with the setup time, $t_{su(A)}$, requirements before the first rising edge of the I/O clock. The multiplexer address is shifted in on the first three rising edges of the I/O clock.

The first seven falling edges of I/O CLOCK shift out the remaining seven bits of the previous conversion on DATA OUT. The eighth I/O clock falling edge returns the MSB to the Data Out. Optimum serial transfer takes place with the bit streams being read on the rising edges of the I/O clock for the respective devices and the Data Out and Address In lines.

At the fourth falling edge of the I/O clock, the on-chip sample-and-hold begins to acquire the newly addressed analog input and continues until the eighth (and final) falling edge. A hold function is initiated by the eighth I/O clock pulse falling edge. To start the conversion at a specific point in time (or lengthen the acquisition time), the host processor may leave the eighth I/O clock pulse in the high state until the moment at which the analog signal must be sampled. After bringing the eighth I/O pulse low, the A/D function is performed in the next 36 internal system clock cycles.

In applications where $\overline{CS}$ is held low continuously, the bursts of eight I/O clock pulses should be timed to be at least t_{conv} apart.

$\overline{CS}$ input

To minimize bus contention caused by noise enabling the 3-state Data Out, when the $\overline{CS}$ input is brought low, the device waits for two rising edges and a falling edge of the internal system clock before recognizing the $\overline{CS}$ transition. Hence, the setup time $t_{su(CS)}$ should be observed when using the $\overline{CS}$ input. This also applies to a $\overline{CS}$ high-to-low transition, except for disabling DATA OUT, which goes into a high-impedance state immediately within the t_{dis} specification (see Figure 3). If this interruption of $\overline{CS}$ in the low state is less than 1.5 internal system clock cycles, and hence not recognized, DATA OUT will be immediately enabled with the return of $\overline{CS}$ to the low state. DATA OUT becomes enabled after a $\overline{CS}$ high-to-low transition in time t_{en} (equivalent to $t_{su(CS)}$ for this device).

$\overline{CS}$ can be brought high during a conversion without affecting the ongoing conversion but must remain high until the end of conversion. Otherwise, a $\overline{CS}$ falling edge causes a reset condition that aborts the conversion in progress. When a new access cycle starts, the previous conversion result is output.

A new conversion may be restarted by toggling $\overline{CS}$ high-to-low at least $t_{su(CS)}$ before the eighth falling edge of the I/O clock. The ongoing access cycle is aborted. Again, when a new access cycle starts, the previous conversion result is output.

end of conversion output (EOC)

EOC goes low at propagation delay time, $t_{PHL(EOC)}$, after the 8th falling edge of the I/O clock and goes high when conversion is complete. At this time, the MSB is available at Data Out; however, if $\overline{CS}$ is high, it is necessary to bring $\overline{CS}$ low and wait for the $\overline{CS}$ recognition time before Data Out is available, since Data Out is in a high-impedance state when $\overline{CS}$ is high. Delay time, $t_{d(EOC)}$, of EOC to Data Out is a negative value of 4 internal system clock cycles less internal propagation delay because the EOC signal is output after 40 internal system clock cycles, whereas conversion is complete with data available after 36 cycles.

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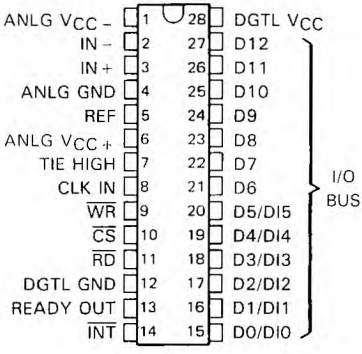
D2982, FEBRUARY 1987 – REVISED JANUARY 1989

- Advanced LinCMOS™ Technology
- Self-Calibration Eliminates Expensive Trimming at Factory and Offset Adjustment in the Field
- 12-Bit Plus Sign Bipolar or 12-Bit Unipolar
- ±1/2 and ±1 LSB Linearity Error in Unipolar Configuration
- 10 µs Conversion Time (clock = 2.6 MHz)
- Compatible with All Microprocessors
- True Differential Analog Voltage Inputs
- 0 to 5 V Analog Voltage Range with Single 5-V Supply (Unipolar Configuration)
- −5 V to 5 V Analog Voltage Range with ±5-V Supplies (Bipolar Configuration)
- Low Power . . . 25 mW Maximum

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The TLC1225A and TLC1225B converters are manufactured with Texas Instruments highly efficient Advanced LinCMOS™ technology. Either of the TLC1225A or TLC1225B CMOS analog-to-digital converters can be operated as a unipolar or bipolar converter. A unipolar input(0 to 5 V) can be accommodated with a single 5-V supply; a bipolar input (−5 V to 5 V) requires the addition of a 5-V negative supply. Conversion is performed via the successive-approximation method. The TLC1225A and TLC1225B output the converted data in a parallel word and interfaces directly to a 16-bit data bus. Negative numbers are given in the two's complement data format. All digital signals are fully TTL and CMOS compatible.

These converters utilize a self-calibration technique by which seven of the internal capacitors in the capacitive ladder of the A/D conversion circuitry can be automatically calibrated. The internal capacitors are calibrated during a nonconversion, capacitor-calibrate cycle in which all seven of the internal capacitors are calibrated at the same time. A conversion requires only 10 µs (2.6 MHz clock) after the nonconversion, capacitor-calibrating cycle has been completed. The calibration or conversion cycle may be initiated at any time by issuing the proper command word to the data bus. The self-calibrating technique eliminates the need for expensive trimming of thin-film resistors at the factory and provide excellent performance at low cost.

The TLC1225AM and TLC1225BM are characterized for operation over the full military temperature range of −55°C to 125°C. The TLC1225AI and TLC1225BI are characterized for operation from −40°C to 85°C.

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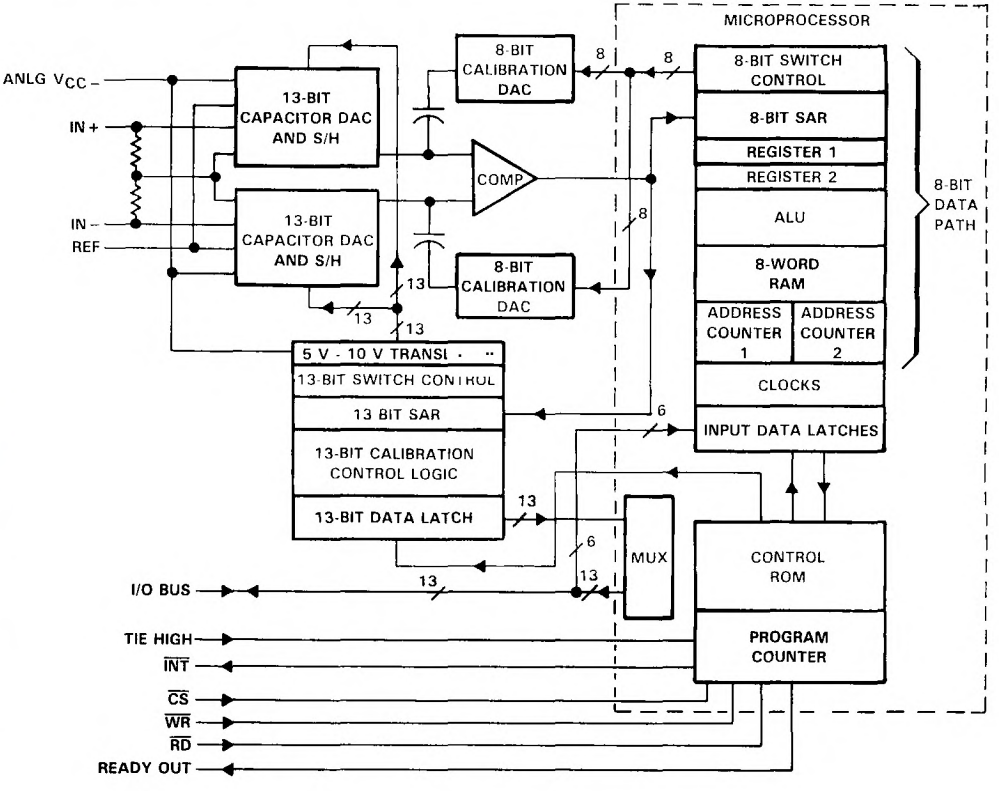
functional block diagram



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operation description

calibration of comparator offset

The following actions are performed to calibrate the comparator offset:

1. The IN+ and IN− inputs are internally shorted together in order that the comparator input is zero. A course comparator offset calibration is performed by storing the offset voltages of the interconnecting comparator stages on the coupling capacitors that connect these stages. Refer to Figure 1. The storage of offset voltages is accomplished by closing all switches and then opening switches A and A′, then switches B and B′, and then C and C′. This process continues until all interconnecting stages of the comparator are calibrated. After this action, some of the comparator offset still remains uncalibrated.

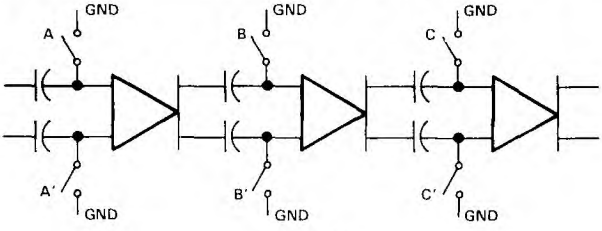

FIGURE 1

2. An A/D conversion is done on the remaining offset with the 8-bit calibration DACs and 8-bit SAR and the result is stored in the RAM.

capacitor calibration of the ADC's capacitive ladder

The following actions are performed to calibrate capacitors in the 13-bit DACs that comprise the ADC's capacitive ladder:

1. The IN+ and IN− inputs are internally disconnected from the 13-bit capacitive DACs.
2. The most significant bit (MSB) capacitor is tied to REF, while the rest of the ladder capacitors are tied to GND. The A/D conversion result for the remaining comparator offset, obtained in Step 2 above, is retrieved from the RAM and is input to the 8-bit DACs.
3. Step 1 of the Calibration of Comparator Offset sequence is performed. The 8-bit DAC input is returned to zero and the remaining comparator offset is then subtracted. Thus, the comparator offset is completely corrected.
4. Now the MSB capacitor is tied to GND, while the rest of the ladder capacitors, C_X, are tied to REF. An MSB capacitor voltage error (see Figure 2) on the comparator output will occur if the MSB capacitor does not equal the sum of the other capacitors in the capacitive ladder. This error voltage is converted to an 8-bit word from which a capacitor error is computed and stored in the RAM.
5. The capacitor voltage error for the next most significant capacitor is calibrated by keeping the MSB capacitor grounded and then performing the above Steps 1-4 while using the next most significant capacitor in lieu of the MSB capacitor. The seven most significant capacitors can be calibrated in this manner.

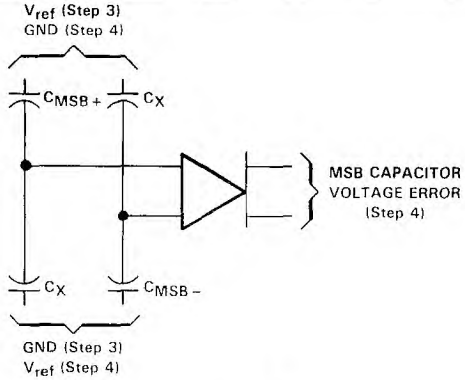

FIGURE 2

analog-to-digital conversion

The following steps are performed in the analog-to-digital conversion process:

1. Step 1 of the Calibration of Comparator Offset Sequence is performed. The A/D conversion result for the remaining comparator offset, which was obtained in Step 2 of the Calibration of Comparator Offset, is retrieved from the RAM and is input to the 8-bit DACs. Thus the comparator offset is completely corrected.
2. IN+ and IN− are sampled onto the 13-bit capacitive ladders.
3. The 13-bit analog-to-digital conversion is performed. As the successive-approximation conversion proceeds successively through the seven most significant capacitors, the error for each of these capacitors is recovered from the RAM and accumulated in a register. This register controls the 8-bit DACs so the total accumulated error for these capacitors is subtracted out during the conversion process.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (ANLG V_{CC+} and DGTL V_{CC}) (see Note 1) . . . . . 15 V
Supply voltage, ANLG V_{CC-} . . . . . −15 V
Control and Clock input voltage range . . . . . −0.3 V to +15 V
Analog input (IN+, IN−) voltage range,
V_{I+} and V_{I-} . . . . . ANLG V_{CC-} −0.3 V to ANLG V_{CC+} +0.3 V
Reference voltage range, V_{ref} . . . . . −0.3 V to ANLG V_{CC+} +0.3 V
Pin 7 voltage range, V_{OS} . . . . . −0.3 V to ANLG V_{CC+} +0.3 V
Output voltage range . . . . . −0.3 V to DGTL V_{CC} +0.3 V
Input current (per pin) . . . . . ±5 mA
Input current (per package) . . . . . ±20 mA
Operating free-air temperature range:
TLC1225AM, TL1225BM . . . . . −55°C to 125°C
TLC1225AI, TLC1225BI . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: N package . . . . . 260°C

NOTE 1: All analog voltages are referred to ANLG GND and all digital voltages are referred to DGTL GND.

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recommended operating conditions

		MIN	MAX	UNIT
Supply voltage	ANLG V_{CC+}	4.5	6	V
	ANLG V_{CC-}	−5.5	ANLG GND	
	DGTL V_{CC}	4.5	6	
High-level input voltage, V_{IH}, all digital inputs except CLK IN (V_{CC} = 4.75 V to 5.25 V)		2		V
Low-level input voltage, V_{IL}, all digital inputs except CLK IN (V_{CC} = 4.75 V to 5.25 V)			0.8	V
Analog input voltage, V_{I+}, V_{I-}	Bipolar range	ANLG V_{CC-} − 0.05	ANLG V_{CC+} + 0.05	V
	Unipolar range	ANLG GND − 0.05	ANLG V_{CC+} + 0.05	
Pin 7 (TIE HIGH)		2		V
Clock input frequency, f_{clock}		0.3	2.6	MHz
Clock duty cycle		40%	60%	
Pulse duration, $\overline{CS}$ and $\overline{WR}$ both low, t_w ($\overline{CS}$·$\overline{WR}$)		50		ns
Setup time before $\overline{WR}$↑ or $\overline{CS}$↑, t_{su}			50	ns
Hold time after $\overline{WR}$↑ or $\overline{CS}$↑, t_h			50	ns
Operating free-air temperature, T_A	TLC1225AM, TLC1225BM	−55	125	°C
	TLC1225AI, TLC1225BI	−40	85	

electrical characteristics over recommended operating free-air temperature range, ANLG V_{CC+} = DGTL V_{CC} = V_{ref} = 5 V, ANLG V_{CC-} = −5 V (for bipolar input range), ANLG V_{CC-} = ANLG GND (for unipolar input range) (unless otherwise noted) (see Note 2)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	DGTL V_{CC} = 4.75 V	I_O = −1.8 mA	2.4		V
			I_O = −50 µA	4.5		
V_{OL}	Low-level output voltage	DGTL V_{CC} = 4.75 V,	I_O = 8 mA		0.4	V
V_{T+}	Clock positive-going threshold voltage			2.7	3.5	V
V_{T-}	Clock negative-going threshold voltage			1.4	2.1	V
V_{hys}	Clock input hysteresis	V_{T+} min − V_{T-} max		0.6		V
		V_{T+} max − V_{T-} min			2.1	
r_{ref}	Input resistance, REF terminal			1	10	MΩ
I_{IH}	High-level input current	V_I = 5 V			1	µA
I_{IL}	Low-level input current	V_I = 0			−1	µA
I_{OZ}	High-impedance-state output leakage current	V_O = 0			−3	µA
		V_O = 5 V			3	
I_O	Output current	V_O = 0			−6	mA
		V_O = 5 V			8	
DGTL I_{CC}	Supply current from DGTL V_{CC}	f_{clk} = 2.6 MHz,	$\overline{CS}$ high		3	mA
ANLG I_{CC+}	Supply current from ANLG V_{CC+}	f_{clk} = 2.6 MHz,	$\overline{CS}$ high		3	mA
ANLG I_{CC-}	Supply current from ANLG V_{CC-}	f_{clk} = 2.6 MHz,	$\overline{CS}$ high		−3	mA

NOTE 2. Bipolar input range is defined as: V_{I+} = −5.05 V to 5.05 V, V_{I-} = −5.05 V to 5.05 V, and $|V_{I+} - V_{I-}| \leq 5.05$ V. The unipolar input voltage range is defined as: V_{I+} = −0.05 V to 5.05 V, V_{I-} = −0.05 V to 5.05 V, and $|V_{I+} - V_{I-}| \leq 5.05$ V.

operating characteristics over recommended operating free-air temperature range, ANLG V_{CC+} = DGTL V_{CC} = V_{ref} = 5 V, ANLG V_{CC-} = −5 V (for bipolar input range), ANLG V_{CC-} = ANLG GND (for unipolar input range), f_{clock} = 2.6 MHz (unless otherwise noted) (see Note 2)

PARAMETER			TEST CONDITIONS		MIN	MAX	UNIT
E_L	Linearity error		Unipolar input range	TLC1225A		±1	LSB
				TLC1225B		±0.5	
			Bipolar input range	TLC1225A		±2	
				TLC1225B		±1.5	
	Zero error					±0.5	LSB
	Adjusted positive and negative full-scale error (see Note 3)		Unipolar input range			±1	LSB
	Adjusted positive and negative full-scale error (see Note 4)		Bipolar input range			±1	LSB
	Temperature coefficient of gain					15	ppm/°C
	Temperature coefficient of offset point					1.5	ppm/°C
k_{SVS}	Supply voltage sensitivity	Zero error	ANLG V_{CC+} = 5 V ± 5%, ANLG V_{CC-} = −5 V ± 5%, DGTL V_{CC} = 5 V ± 5%			±0.75	LSB
		Positive and negative full-scale error				±0.75	
		Linearity error				±0.25	
t_c	Conversion time ($1/f_{clk}$)					27	clock cycles
t_a	Access time (delay from falling edge of $\overline{CS}$·$\overline{RD}$ to data output)		C_L = 100 pF			110	ns
t_{dis}	Disable time, output (delay from rising edge of $\overline{RD}$ to high-impedance state		R_L = 10 kΩ,	C_L = 10 pF		60	ns
			R_L = 2 kΩ,	C_L = 100 pF		60	
$t_{d(READY)}$	$\overline{RD}$ or $\overline{WR}$ to READY OUT delay					140	ns
$t_{d(INT)}$	$\overline{RD}$ or $\overline{WR}$ to reset of $\overline{INT}$ delay					400	ns

NOTES: 2. Bipolar input range is defined as: V_{I+} = −5.05 V to 5.05 V, V_{I-} = −5.05 V to 5.05 V, and $|V_{I+} - V_{I-}| \leq 5.05$ V. The unipolar input voltage range is defined as: V_{I+} = −0.05 V to 5.05 V, V_{I-} = −0.05 V to 5.05 V, and $|V_{I+} - V_{I-}| \leq 5.05$ V.

3. See the Positive and Negative Full-Scale Adjustment section, Unipolar Inputs.

4. See the Positive and Negative Full-Scale Adjustment section, Bipolar Inputs

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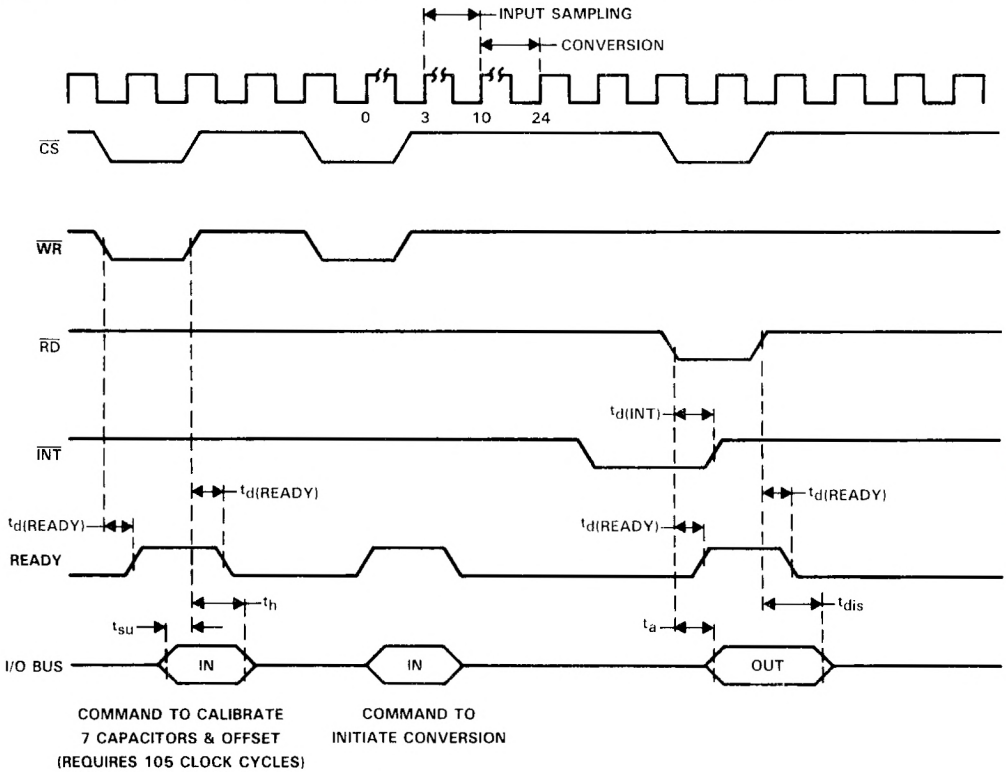

FIGURE 3. TIMING DIAGRAM

PARAMETER MEASUREMENT INFORMATION

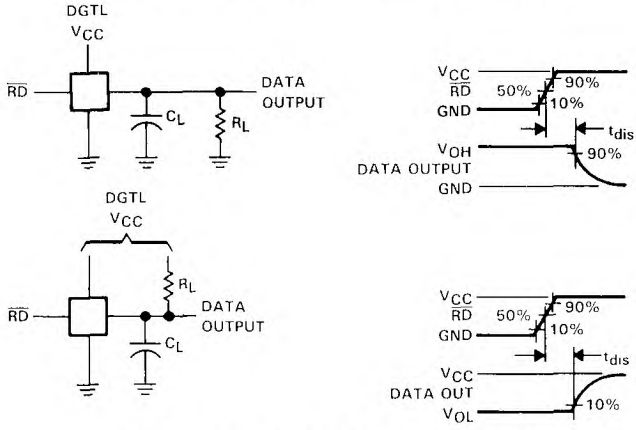

FIGURE 4. LOAD CIRCUITS AND WAVEFORMS

PRINCIPLES OF OPERATION

power-up calibration sequence

Power-Up calibration is not automatic and calibration is initiated by writing control words to the six least significant bits of the data bus. If addressed or initiated, conversion can begin after the first clock cycle. However, full A/D conversion accuracy is not established until after internal capacitor calibration.

conversion start sequence

The writing of the conversion command word to the six least significant bits of the data bus, when either $\overline{CS}$ or $\overline{WR}$ goes high, initiates the conversion sequence.

analog sampling sequence

Sampling of the input signal occurs during clock cycles 3 thru 10 of the conversion sequence.

completed A/D conversion

When $\overline{INT}$ goes low, conversion is complete and the A/D result can be read. A new conversion can begin immediately. The A/D conversion is complete at the end of clock cycle 27 of the conversion sequence.

aborting a conversion in process and beginning a new conversion

If a conversion is initiated while a conversion sequence is in process, the ongoing conversion will be aborted and a new conversion sequence will begin.

reading the conversion result

When both $\overline{CS}$ and $\overline{RD}$ go low, all 13 bits of conversion data are output to the I/O bus. The format of the output is extended sign with 2's complement, right justified data. For both unipolar and bipolar cases, the sign bit D12 is low if $V_{I+} - V_{I-}$ is positive and high if $V_{I+} - V_{I-}$ is negative.

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general

reset INT

When reading the conversion data, the falling edge of the first low-going combination of $\overline{CS}$ and $\overline{RD}$ will reset $\overline{INT}$. The falling edge of the low-going combination of $\overline{CS}$ and $\overline{WR}$ will also reset $\overline{INT}$.

ready out

For high-speed microprocessors, READY OUT allows the TLC1225 to insert a wait state in the microprocessor's read or write cycle.

reference voltage (V_{ref})

This voltage defines the range for $|V_{I+} - V_{I-}|$. When $|V_{I+} - V_{I-}|$ equals V_{ref}, the highest conversion data value results. When $|V_{I+} - V_{I-}|$ equals 0, the conversion data value is zero. Thus, for a given input, the conversion data changes ratiometrically with changes in V_{ref}.

TIE HIGH

This pin is a digital input and should be tied high.

calibration and conversion considerations

Calibration of the internal capacitor and A/D conversion are two separate actions. Each action is independently initiated. A calibration command that calibrates all seven internal capacitors is normally issued before conversion. A conversion command then initiates the A/D conversion. Subsequent conversions can be performed by issuing additional conversion commands. The calibration and conversion commands are totally independent from one another and can be initiated in any order. Calibration and conversion commands require 105 and 27 clock cycles, respectively.

The calibrate and conversion commands are initiated by writing control words on the six least significant bits of the data bus. These control words are written into the IC when either $\overline{CS}$ or $\overline{WR}$ goes high. The initiation of these commands is illustrated in the Timing Diagram. The bit patterns for the commands are shown in Table 1.

TABLE 1. CONVERSION COMMANDS

COMMAND	$\overline{CS}$ + $\overline{WR}$	I/O BUS						REQUIRED NUMBER OF CLOCK CYCLES
		DI5	DI4	DI3	DI2	DI1	DI0	
Conversion	↑	H	L	X	X	X	L	27
Calibrate†	↑	L	X	L	L	L	L	105

†Calibration is lost when clock is stopped.

analog inputs

differential inputs provide common-mode rejection

The differential inputs reduce common-mode noise. Common-mode noise is noise common to both IN+ and IN− inputs, such as 60-Hz noise. There is no time interval between the sampling of the IN+ and IN− so these inputs are truly differential. Thus, no conversion errors result from a time interval between the sampling of the IN+ and IN− inputs.

input bypass capacitors

Input bypass capacitors may be used for noise filtering. However, the charge on these bypass capacitors will be depleted during the input sampling sequence when the internal sampling capacitors are charged. Note that the charging of the bypass capacitors through the differential source resistances must keep pace with the charge depletion of the bypass capacitors during the input sampling sequence. Higher source resistances reduce the amount of charging current for the bypass capacitors. Also, note that fast, successive conversion

will have the greatest charge depletion effect on the bypass capacitors. Therefore, the above phenomenon becomes more significant as source resistances and the converssion rate (i.e., higher clock frequency and conversion initiation rate) increase.

In addition, if the above phenomenon prevents the bypass capacitors from fully charging between conversions, voltage drops across the source resistances will result due to the ongoing bypass capacitor charging currents. The voltage drops will cause a conversion error. Also, the voltage drops increase with higher $|V_{I+} - V_{I-}|$ values, higher source resistances, and lower charge on the bypass capacitors (i.e., faster conversion rate).

For low-source-resistance applications ($R_{source} < 100\ \Omega$), a 0.001-μF bypass capacitor at the inputs will prevent pickup due to the series lead inductance of a long wire. A 100-Ω resistor can be placed between the capacitor and the output of an operational amplifier to isolate the capacitor from the operational amplifier.

input leads

The input leads should be kept as short as possible, since the coupling of noise and digital clock signals to the inputs can cause errors.

power supply considerations

Noise spikes on the V_{CC} lines can cause conversion error. Low-inductance tantalum capacitors (> 1 μF) with short leads should be used to bypass ANLG V_{CC} and DGTL V_{CC}. A separate regulator for the TLC1225A or TLC1225B and other analog circuitry will greatly reduce digital noise on the supply line.

positive and negative full-scale adjustment

unipolar inputs

Apply a differential input voltage that is 0.5 LSB below the desired analog full-scale voltage (V_{FS}) and adjust the magnitude of the REF input so that the output code is just changing from 0 1111 1111 1110 to 0 1111 1111 1111. If this transition is desired for a different input voltage, the reference voltage can be adjusted accordingly.

bipolar inputs

First, follow the procedure for the unipolar case.

Second, apply a differential input voltage so that the digital output code is just changing from 1 0000 0000 0001 to 1 0000 0000 0000. Call this actual differential voltage V_X. The ideal differential voltage for this transition is:

$$-V_{FS} + \frac{V_{FS}}{8192} \tag{1}$$

The difference between the actual and ideal differential voltages is:

$$\text{Delta} = V_X - \left(-V_{FS} + \frac{V_{FS}}{8192}\right) \tag{2}$$

Then apply a differential input voltage of:

$$V_X - \frac{\text{Delta}}{2} \tag{3}$$

and adjust V_{ref} so the digital output code is just changing from 1 0000 0000 0001 to 1 0000 0000 0000. This procedure produces positive and negative full-scale transitions with symmetrical minimum error.

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TYPICAL APPLICATIONS

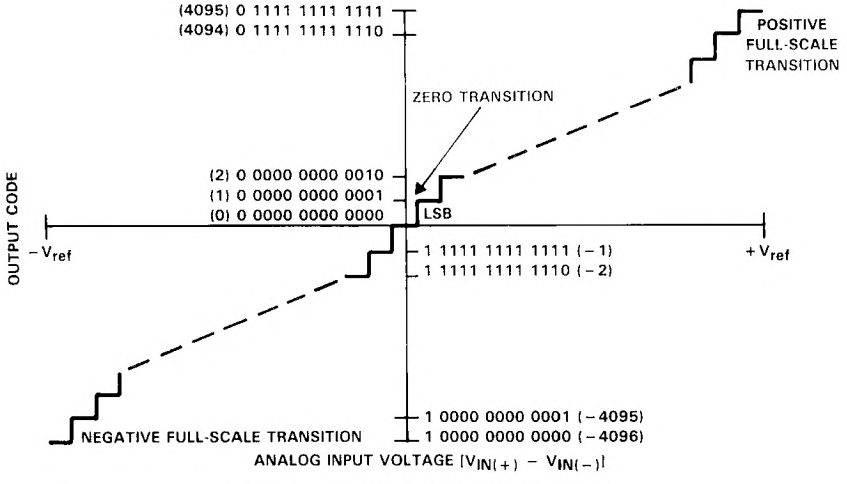
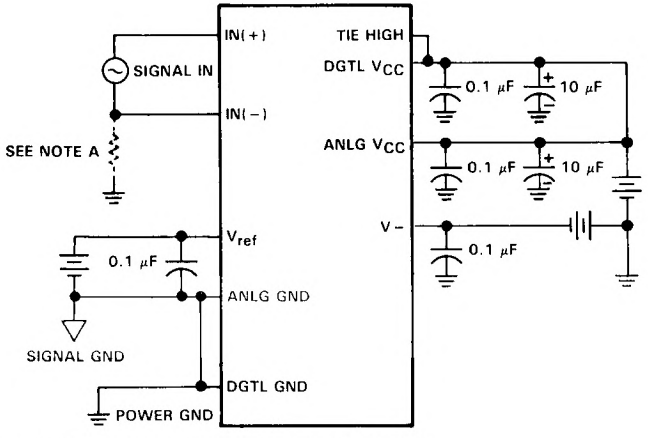


FIGURE 5. TRANSFER CHARACTERISTIC



NOTES: A The analog input must have some current return path to ANALOG GND.
B. Bypass capacitor leads must be as short as possible.

FIGURE 6. ANALOG CONSIDERATIONS

TYPICAL APPLICATIONS (Continued)

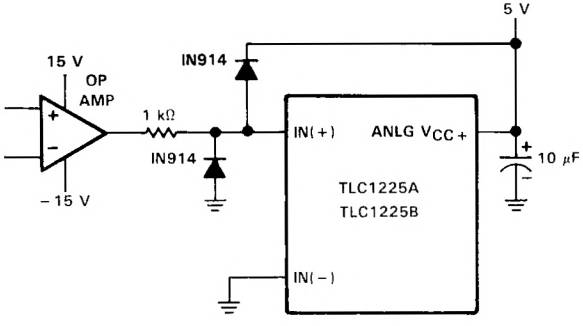
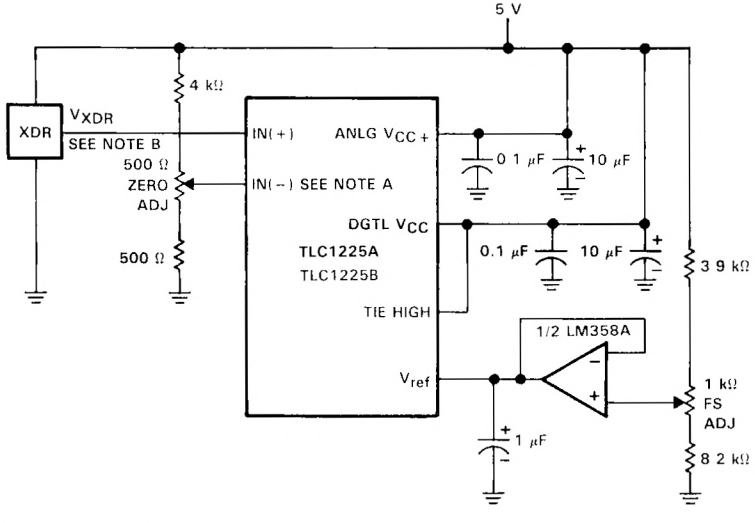


FIGURE 7. INPUT PROTECTION



NOTES: A. $V_{I-} = 0.15 \times$ ANLG V_{CC+}.
B. 15% of ANALOG $V_{CC} \leq V_{XDR} \leq$ 85% of ANALOG V_{CC}

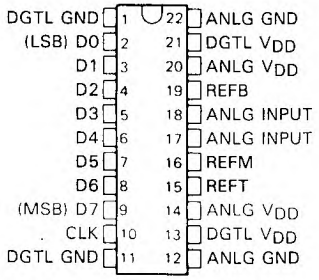
FIGURE 8. OPERATING WITH RATIOMETRIC TRANSDUCERS

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D3220, ARY 1989

- 8-Bit Resolution
- 0.2% Linearity
- Maximum Conversion Rate . . . 25 MHz Typ
  20 MHz Min
- Analog Input Voltage Range . . .
  V_{CC} to V_{CC} – 2 V
- Analog Input Dynamic Range . . . 2 V to 5 V
- TTL Digital I/O Level
- Low Power Consumption . . . 200 mW Typ
- 5-V Single-Supply Operation
- Interchangeable with Fujitsu MB40578

N PACKAGE
(TOP VIEW)

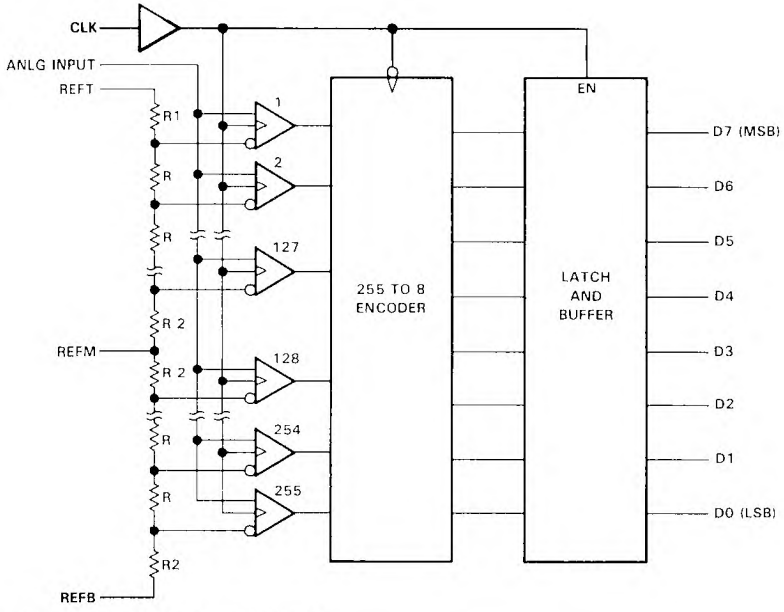


description

The TLC5502 is a low-power ultra-high-speed video-band analog-to-digital converter that uses the LinEPIC™ 1-μm CMOS process. It utilizes the full-parallel comparison (flash method) for high-speed conversion. It converts wide-band analog signals (such as a video signal) to a digital signal at a sampling rate of dc to 30 MHz. Because of such high-speed capability, the TL5502 is suitable for digital video applications such as digital TV, video processing with a computer, or radar signal processing.

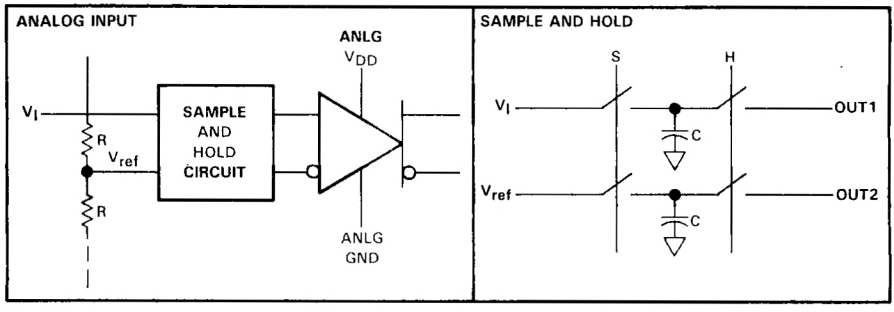
The TL5502 is characterized for operation from 0°C to 70°C.

functional block diagram

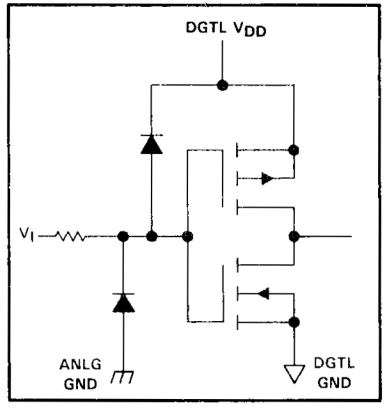


LinEPIC is a trademark of Texas Instruments Incorporated.

equivalents of analog input circuit



equivalent of digital input circuit



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

FUNCTION TABLE

STEP	ANALOG INPUT VOLTAGE†	DIGITAL OUTPUT CODE
0	2.960 V	L L L L L L L L
1	2.968 V	L L L L L L L H
⋮	⋮	⋮
127	3 976 V	L H H H H H H H
128	3 984 V	H L L L L L L L
129	3.992 V	H L L L L L L H
⋮	⋮	⋮
254	4.992 V	H H H H H H H L
255	5.000 V	H H H H H H H H

†These values are based on the assumption that V_{refB} and V_{refT} have been adjusted so that the voltage at the transition from digital 0 to 1 (V_{ZT}) is 2.964 V and the transition to full scale (V_{FT}) is 4 996 V. 1 LSB = 8 mV.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, ANLG V_{DD} . . . . . −0.5 V to 7 V
Supply voltage range, DGTL V_{DD} . . . . . −0.5 V to 7 V
Input voltage range at digital input, V_I . . . . . −0.5 V to 7 V
Input voltage range at analog input, V_I . . . . . −0.5 V to ANLG V_{DD} + 0.5 V
Analog reference voltage range, V_{ref} . . . . . −0.5 V to ANLG V_{DD} + 0.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, ANLG V_{DD}	4.75	5	5.25	V
Supply voltage, DGTL V_{DD}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Input voltage at analog input, V_I	0		5	V
Analog reference voltage (top side), V_{refT}	3		ANLG GND	V
Analog reference voltage (bottom side), V_{refB}	ANLG GND		3	V
Differential reference voltage, $V_{refT} - V_{refB}$	2		5	V
High-level output current, I_{OH}			−400	μA
Low-level output current, I_{OL}			4	mA
Clock pulse duration, high-level or low-level, t_w	25			ns
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over operating supply voltage range, T_A = 25°C (unless otherwise noted)

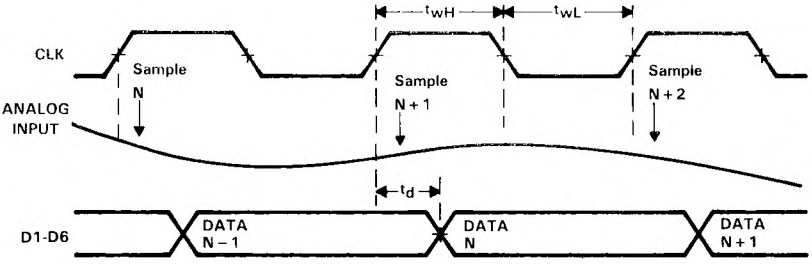
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −400 μA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA			0.4	V
I_I	Analog input current	V_I = 4 V			15	μA
I_{IH}	Digital high-level input current	V_I = 5 V			1	μA
I_{IL}	Digital low-level input current	V_I = 0			−1	μA
I_I	Digital input current	V_I = 7 V			100	μA
I_{refB}	Reference current	V_{refB} = 3 V		−10		mA
I_{refT}	Reference current	V_{refT} = 5 V		−10		mA
r_i	Analog input resistance		1			MΩ
C_i	Analog input capacitance			50	75	pF
I_{CC}	Supply current			40	60	mA

operating characteristics over operating supply voltage range, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
E_L	Linearity error				±0.2	%FSR
f_{max}	Maximum conversion rate		20	30		MHz
t_d	Digital output delay time	See Figure 3		15	30	ns

3 Product Previews

timing diagram



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

TYPICAL CHARACTERISTICS

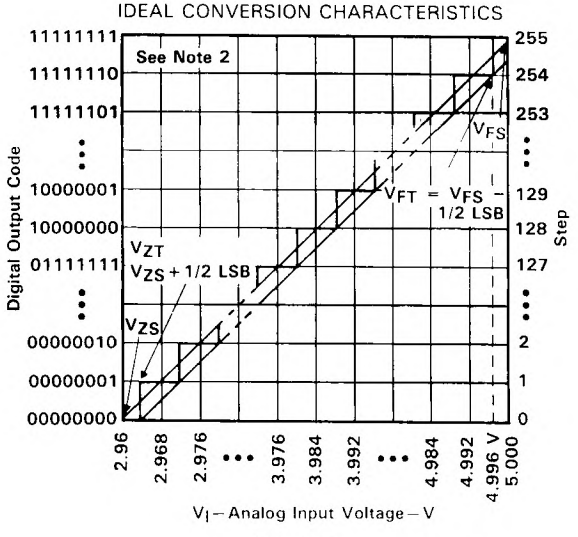


FIGURE 1

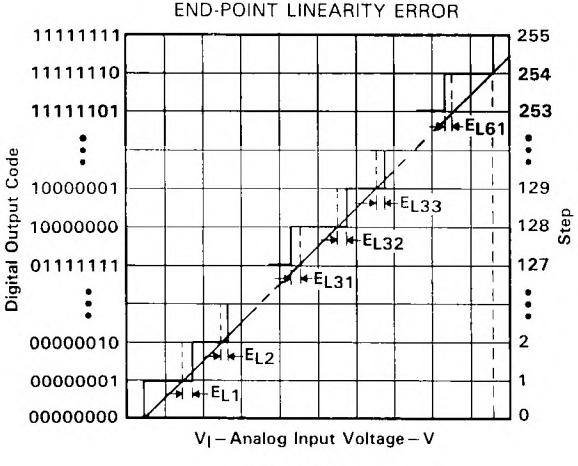


FIGURE 2

NOTE 2: This curve is based on the assumption that V_{refB} and V_{refT} have been adjusted so that the voltage at the transition from digital 0 to 1 (V_{ZT}) is 4.000 V and the transition to full scale (V_{FT}) is 4.992 V. 1 LSB = 16 mV.

PARAMETER MEASUREMENT INFORMATION

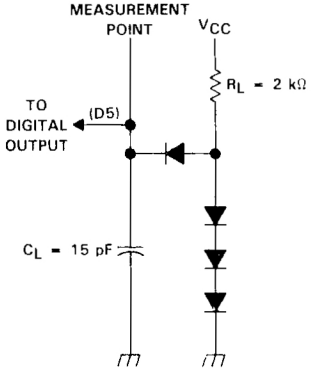


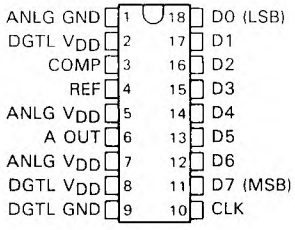
FIGURE 3. LOAD CIRCUIT

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D3224, FEBRUARY 1989

- 8-Bit Resolution
- ±0.2% Linearity
- Maximum Conversion Rate . . .
  30 MHz Typ
  20 MHz Min
- Analog Output Voltage Range of V_{CC} to V_{CC} – 1 V
- TTL Digital Input Voltage
- 5-V Single Power Supply Operation
- Low Power Consumption . . .
  80 mW Typical
- Interchangeable with Fujitsu MB40778

N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The TLC5602 is a low-power ultra-high speed video digital-to-analog converter that uses the LinEPIC™ 1-μm CMOS process. The TL5602 converts digital signals to analog signals at a sampling rate of dc to 20 MHz. Because of high-speed operation, the TLC5602 is suitable for digital video applications such as digital television, video processing with a computer, and radar-signal processing.

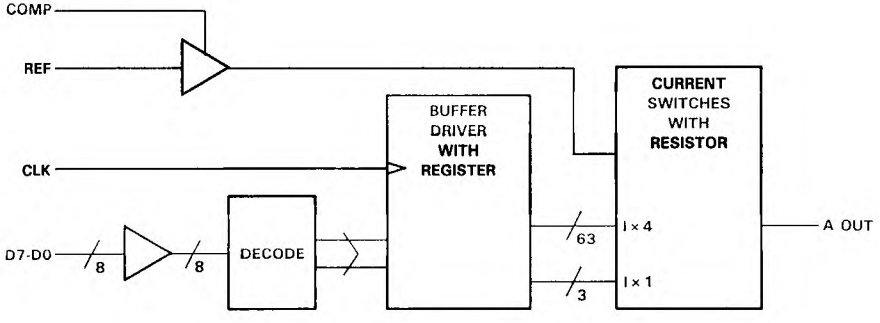
The TLC5602 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

STEP	DIGITAL INPUTS								OUTPUT
	D7	D6	D5	D4	D3	D2	D1	D0	VOLTAGE†
0	L	L	L	L	L	L	L	L	3.980 V
1	L	L	L	L	L	L	L	H	3.984 V
⋮					⋮				⋮
127	L	H	H	H	H	H	H	H	4.488 V
128	H	L	L	L	L	L	L	L	4 492 V
129	H	L	L	L	L	L	L	H	4.496 V
⋮					⋮				⋮
254	H	H	H	H	H	H	H	L	4.996 V
255	H	H	H	H	H	H	H	H	5.000 V

†For V_{DD} = 5 V, V_{ref} = 3.976 V.

functional block diagram



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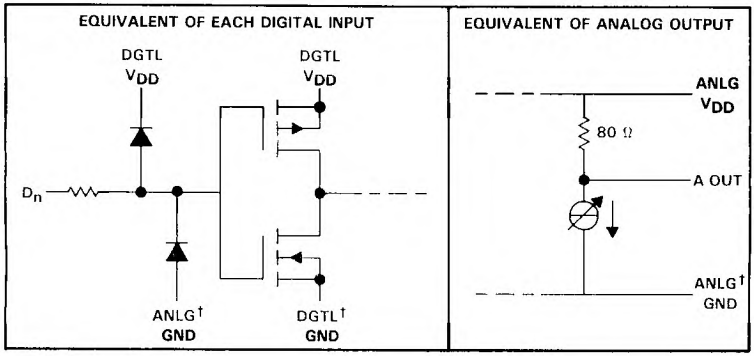
schematic of digital input and analog output



†ANLG GND and DGTL GND are not connected internally and should be tied together as close to the device as possible.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, ANLG V_{DD}, DGTL V_{DD} . . . . . −0.5 V to 7 V
Digital input voltage range, V_I . . . . . −0.5 V to 7 V
Analog reference voltage range, V_{ref} . . . . . 3.5 V to V_{DD}+0.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4.75	5	5.25	V
Analog reference voltage, V_{ref} (see Note 1)	3.8	4	4.2	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Pulse duration, CLK high or low, t_w	25			ns
Setup time, data high before CLK↑, t_{su}	12.5			ns
Hold time, data high after CLK↑, t_h	12.5			ns
Phase compensation capacitance, C_{comp} (see Note 2)	1			μF
Operating free-air temperature, T_A	0		70	°C

NOTES: 1. V_{ref} should be greater than or equal to V_{DD} − 1.2 V.
2. The phase compensation capacitor should be connected between COMP and ANLG GND.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_{IH}	High-level input current	V_{DD} = 5.25 V, V_I = 2.7 V			1	µA
I_{IL}	Low-level input current	V_{DD} = 5.25 V, V_I = 0.4 V			−1	µA
I_{ref}	Input reference current	V_{ref} = 4 V			1	µA
V_{FS}	Full-scale analog output voltage	V_{DD} = 5 V, V_{ref} = 4 V	$V_{DD}-15$	V_{DD}	$V_{DD}+15$	mV
V_{ZS}	Zero-scale analog output voltage		3.919	3.98	4 042	V
r_o	Output resistance	T_A = 25°C	60		100	Ω
C_i	Input capacitance	f_{clock} = 1 MHz, T_A = 25°C		15		pF
I_{DD}	Supply current	V_{ref} = 4.05 V		16	25	mA

operating characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
E_L	Linearity error, best-straight-line				±0.2%	
E_D	rity error, differential				±0.1%	
G_{diff}	ential gain	NTSC 40 IRE modulated ramp,			2%	
ϕ_{diff}	Differential phase	f_{clock} = 14.3 MHz			2°	
t_{pd}	Propagation delay, CLK to analog output	C_L = 10 pF		25		n
t_s	Settling time to within ½LSB	C_L = 10 pF		30		n

†All typical values are at V_{DD} = 5 V and T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

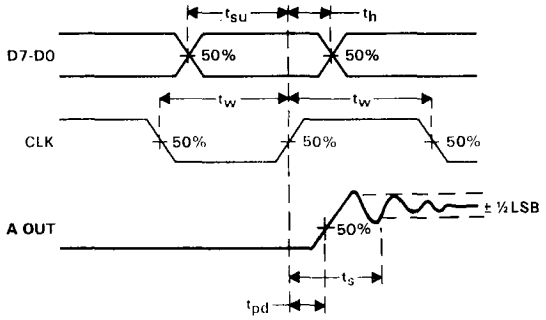


FIGURE 1. VOLTAGE WAVEFORMS

TYPICAL CHARACTERISTICS

IDEAL CONVERSION CHARACTERISTICS

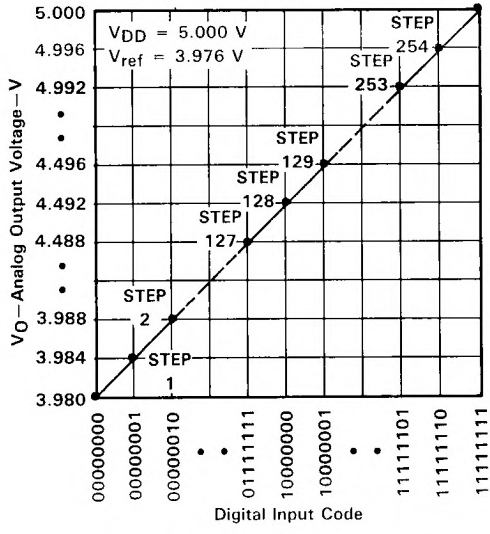


FIGURE 2

BEST-STRAIGHT-LINE LINEARITY ERROR

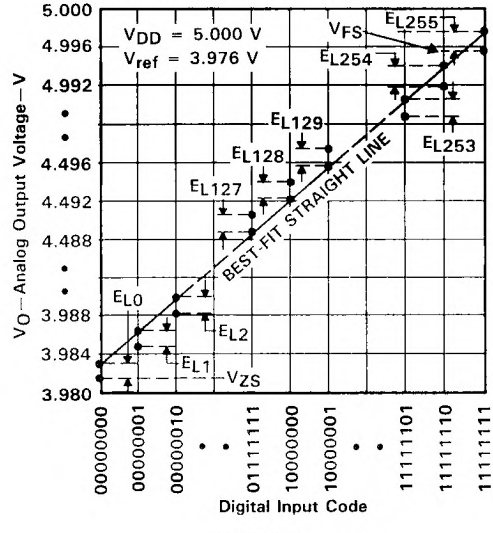


FIGURE 3

TEXAS INSTRUMENTS
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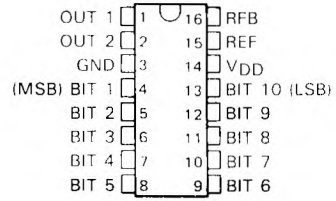
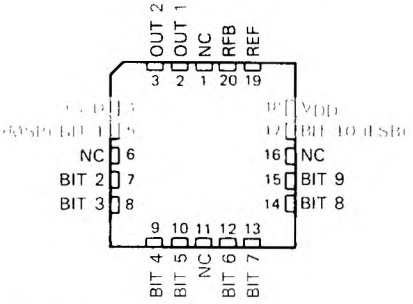
- Advanced LinCMOS™ Silicon-Gate Technology
- Monotonic Over the Entire A/D Conversion Range
- Fast Settling Time
- CMOS/TTL Compatible
- Four-Quadrant Multiplication
- Designed to be Interchangeable with Analog Devices AD7533, AD7520, and PMI PM-7533

KEY PERFORMANCE SPECIFICATIONS	
Resolution	10 Bits
Linearity Error	1/2 LSB
Power Dissipation	30 mW
Settling Time	150 ns

TLC7533 . . . D OR N PACKAGE
AD7533 . . . N PACKAGE
(TOP VIEW)



FN CHIP CARRIER PACKAGE
(TOP VIEW)



NC—No internal connections

description

The TLC7533 and AD7533 are Advanced LinCMOS™ 10-bit digital-to-analog converters featuring two- and four-quadrant multiplication.

The TLC7533 and AD7533 are functionally equivalent to the AD7520 and have the same pinout. Texas Instruments advanced thin-film-on-monolithic-CMOS fabrication process provides 10-bit linearity without laser trimming.

The TLC7533 and AD7533 feature TTL or CMOS compatibility with low input leakage currents from 5-V to 15-V power supplies. Output scaling is provided by an internal feedback resistor and an external operational amplifier. Either positive or negative reference voltages can be used.

The TLC7533C and AD7533I are characterized for operation from −25°C to 85°C. The TLC7533L and AD7533C are characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

SYMBOLIZATION†		OPERATING
DEVICE	PACKAGE SUFFIX	TEMPERATURE RANGE
TLC7533C	D, FN, N	0°C to 70°C
TLC7533I	D, FN, N	−25°C to 85°C
AD7533C	FN, N	−25°C to 85°C
AD7533L	FN, N	0°C to 70°C

† In many instances, these ICs may have both TLC7533 and AD7533 labeling on the package.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . −0.3 V to 17 V
Digital input voltage, V_I . . . . . −0.3 to V_{DD}+0.3 V
Output voltage at T_A = 25°C, OUT1 and OUT2 . . . . . ±25 V
R_{FB} to ground at T_A = 25°C . . . . . −0.3 V to V_{DD}
Reference voltage, V_{ref} . . . . . ±25 V
Operating free-air temperature range: TLC7533I, AD7533C . . . . . −25°C to 85°C
TLC7533C, AD7533L . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C

NOTE 1: All voltage values are with respect to the network ground terminal.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		5		16.5	V
Reference voltage, V_{ref}			±10		V
High-level input voltage, V_{IH}		2.4			V
Low-level input voltage, V_{IL}				0.8	V
Operating free-air temperature, T_A	TLC7533I, AD7533C	−25		85	°C
	TLC7533C, AD7533L	0		70	

electrical characteristics over recommended operating temperature range, V_{DD} = 15 V, V_{ref} = ±10 V, OUT1 and OUT2 at 0 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	MAX	UNIT
I_{Ilkg}	Input leakage current		V_I = 0 or V_{DD}			±1	μA
r_i	Input resistance, REF (see Note 2)				5	20	kΩ
I_{Olkg}	Output leakage current	OUT1	Digital inputs at V_{IL}	Full range		±200	nA
				25°C			
		OUT2	Digital inputs at V_{IH}	Full range		±	
				25°C			
k_{SVS}	Supply voltage sensitivity $\Delta A_V/\Delta V_{DD}$ (see Note 3)		V_{DD} = 14 V to 17 V, Digital inputs at V_{IH} or V_{IL}	Full range		0	%/%
				25°C		0.005	
I_{DD}	Supply current					2	mA
C_i	Input capacitance		V_I = 0 or V_{DD}			5	pF
C_o	Output capacitance	OUT1	Digital inputs at V_{IH}			100	pF
		OUT2				35	
		OUT1	Digital inputs at V_{IL}			35	
		OUT2					

NOTES: 2. Temperature coefficient is approximately −300 ppm/°C.
3. A_V is the ratio of the D/A external operational amplifier output voltage to the REF input voltage when using the internal feedback resistor.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

operating characteristics over recommended operating free-air temperature range, V_{DD} = 15 V, V_{ref} = 10 V, OUT1 and OUT2 at 0 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Relative accuracy	See Note 4			±0.05	%FSR
Gain error	Digital inputs = V_{IH}, See Notes 4 and 5	Full range		±1.5	%FS
		[illegible]		±1.4	
Output current settling time	To ±0.05% FSR, R_L = 100 Ω Digital inputs changing from V_{IH} to V_{IL}, or V_{IL} to V_{IH}			150	ns
Feedthrough error	Digital inputs at V_{IL}, V_{ref} = ±10 V sine wave at 100 kHz			±0.1	%FSR

NOTES 4. Practical Full Scale Range (FSR) = V_{ref} – 1 LSB.
5. Gain error is measured using an internal feedback resistor, Full Scale (FS) = V_{ref} (1023/1024). Maximum gain change from T_A = 25°C to minimum or maximum temperature is ±0.1% FSR.

PRINCIPLES OF OPERATION

The TLC7533 and AD7533 are 10-bit multiplying D/A converters consisting of an inverted R-2R ladder and analog switches. Binary-weighted currents are switched between the OUT1 and OUT2 bus lines by NMOS current switches. The on-state resistances of these switches are binarily scaled so that the voltage drop across every switch is the same. The OUT1 and OUT2 bus lines should be maintained at the same potential so that the current in each ladder leg remains constant and is independent of the switch state. Most applications require only the addition of an external operational amplifier and a voltage reference.

The equivalent circuit for all digital inputs low is shown in Figure 1. With all of the digital inputs low, the entire reference current, I_{ref}, is switched to OUT2 as shown in Figure 2. The current source $I_{ref}/1024$ represents the constant current flowing through the termination resistor of the R-2R ladder; while the current source I_{lkg} represents leakage currents to the substrate. The output capacitances, $C_{o(1)}$ and $C_{o(2)}$, are due to the capacitance of the NMOS current switches and vary with the switch state. With all digital inputs low, all of the current switches and the entire resistor ladder are switched to the OUT2 bus line. The capacitance appearing at OUT2 is a maximum of 100 pF; at OUT1 there is a maximum of 35 pF. With all digital inputs high, all of the current switches are switched to OUT1, and 100 pF maximum appears at OUT1. A maximum of 35 pF appears at OUT2 as shown in Figure 3.

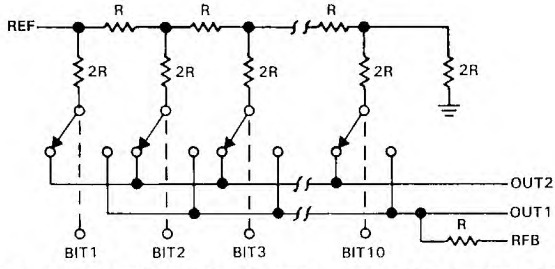

FIGURE 1. SIMPLIFIED D/A CIRCUIT – ALL DIGITAL INPUTS LOW

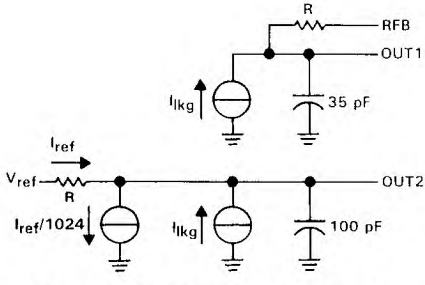

FIGURE 2. D/A EQUIVALENT CIRCUIT – ALL DIGITAL INPUTS LOW

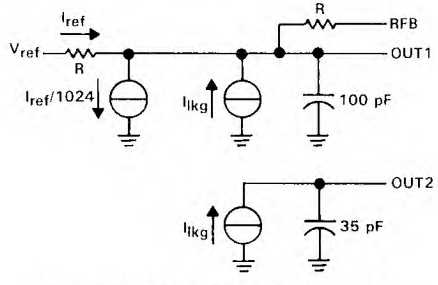

FIGURE 3. D/A EQUIVALENT CIRCUIT – ALL DIGITAL INPUTS HIGH

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TYPICAL APPLICATION DATA

The TLC7533 and AD7533 are capable of performing 2-quadrant or full 4-quadrant multiplication. Circuit configurations for 2-quadrant or 4-quadrant multiplication are shown in Figures 4 and 5. Input coding for unipolar and bipolar operation are summarized in Tables 1 and 2, respectively.

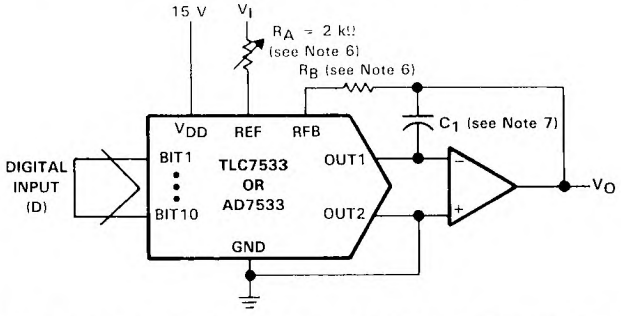


FIGURE 4. UNIPOLAR OPERATION (2-QUADRANT MULTIPLICATION)

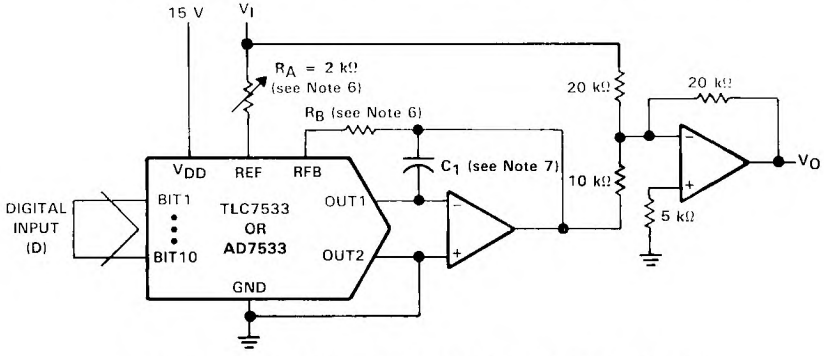


FIGURE 5. BIPOLAR OPERATION (4-QUADRANT OPERATION)

NOTES: 6. R_A and R_B are used only if gain adjustment is required.
7. C_1 (10-33 pF) may be required for phase compensation when using high-speed op-amps

TABLE 1. UNIPOLAR BINARY CODE

DAC DIGITAL INPUT MSB LSB†	ANALOG OUTPUT
1111111111	V_I (1023/1024)
1000000001	$-V_I$ (513/1024)
1000000000	$-V_I$ (512/1024) = $-V_{ref}/2$
0111111111	V_I (511/1024)
0000000001	$-V_I$ (1/1024)
0000000000	$-V_I$ (0/1024) = 0

† 1 LSB $(2^{-10})\ V_I$

TABLE 2. BIPOLAR (OFFSET BINARY) CODE

DAC DIGITAL INPUT MSB LSB‡	ANALOG OUTPUT
1111111111	$+V_I$ (511/512)
1000000001	$+V_I$ (1/512)
1000000000	0
0111111111	$-V_I$ (1/512)
0000000001	$-V_I$ (511/512)
0000000000	$-V_I$ (512/512) = $-V_I$

‡ 1 LSB $(2^{-9})\ V_I$

TYPICAL APPLICATION DATA

The TLC7533 and AD7533 may be used in voltage output operation as shown in Figure 6. In this configuration, the input voltage is applied to the OUT1 terminal and the output voltage is taken from the REF terminal. The output voltage varies with the digital input code according to the equation shown. The output should be buffered to prevent loading errors due to the high output resistance of this circuit (typically 10 kΩ). The input voltage should not exceed 1.5 V to ensure nonlinearity errors less than 1 LSB.

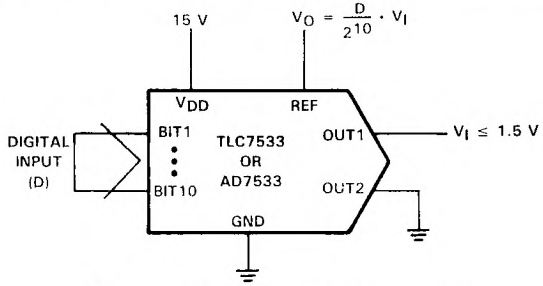
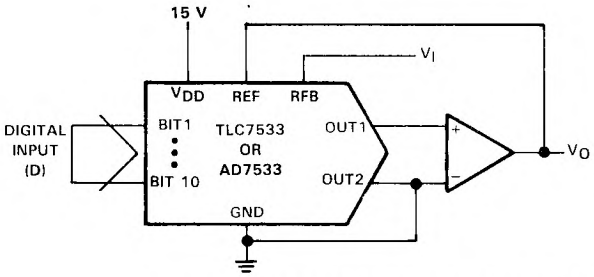


FIGURE 6. VOLTAGE OUTPUT OPERATION

By connecting the DAC in the feedback of an op-amp as shown in Figure 7, the circuit behaves as a programmable gain amplifier with the transfer function:

$$V_O = -V_I \left(\frac{1024}{D}\right)$$

where D = Digital Input Code (expressed as a decimal number)



GAIN TABLE	
D	V_O/V_I
1023	−1.00097
512	2
256	−4
128	−8
2	−512
1	−1024
0	open loop

FIGURE 7. PROGRAMMABLE GAIN AMPLIFIER

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TYPICAL APPLICATION DATA

The programmable function generator shown in Figure 8 produces both square and triangular wave output at a frequency determined by the digital input code. The digital input of the digitally programmable limit detector shown in Figure 9 determines the trip point of the PASS/FAIL output. For a digital input of 00000 00000, the threshold is 0 V, for 11111 11111, the threshold is $-V_{ref}$.

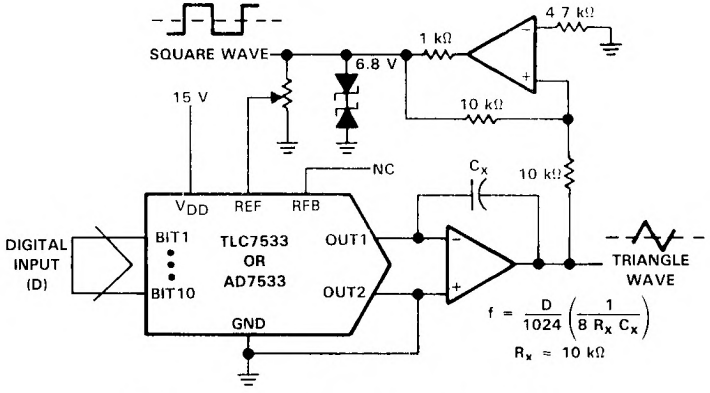

FIGURE 8. PROGRAMMABLE FUNCTION GENERATOR

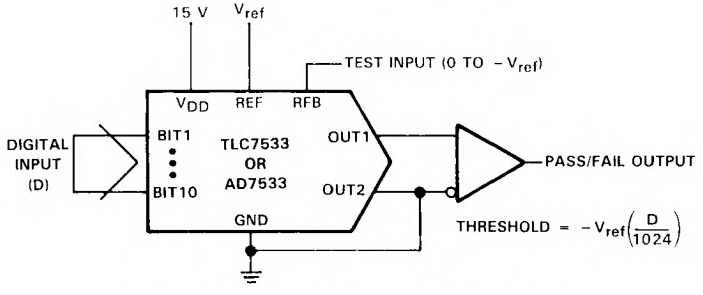

FIGURE 9. PROGRAMMABLE LIMIT DETECTOR

TYPICAL APPLICATION DATA

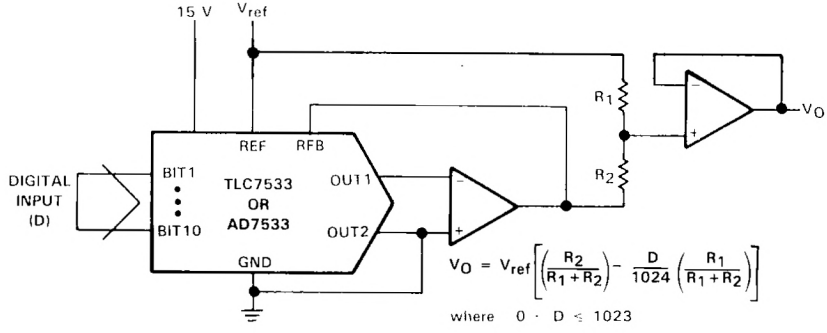

FIGURE 10. MODIFIED SCALE-FACTOR AND OFFSET

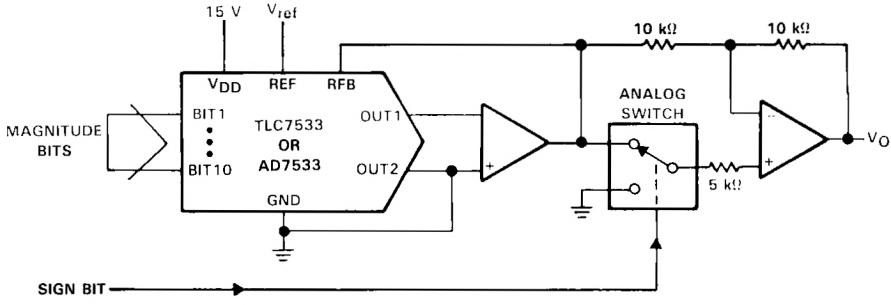

FIGURE 11. 10-BIT AND SIGN MULTIPLYING D/A

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